The Advanced Composition Explorer Mission
California Institute of Technology

ACE-CT-100-22

Environmental Design & Test Requirements for the ACE Payload

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Signature Page

Prepared by:
G. S. Murphy
G. Murphy
Payload System Engineer

Approved by:
Howard W. Eyerly
H. Eyerly
Payload Performance Assurance Mgr.

Reviewed by:
U I von Mehlem 9/22/94
U. I. von Mehlem (note 1)
ACE Spacecraft Systems Engineer

Approved by:
A. Frandsen
A. Frandsen
Payload Manager

Reviewed by:
William B. Cross 9/23/94
W. Cross
ACE System Manager

note 1: Take exception to the R-4.7 requirement: "....thermal design shall assure junction temperatures in flight shall be held to less than 70°C." This requirement is considered very tight compared with the 100°C placed on spacecraft components and may cause instrument hardware weight increases. UIvM

Document Change Log

Revision	Issue Date	CR Reference(s)	Change Pages
Baseline	July 6, 1994		
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1.0 Introduction

1.1 Purpose and Scope

This document provides a comprehensive resource for environment design & compatibility for the ACE payload hardware. It is driven by environments specified in the APL Environmental Specification, (APL-7345-9007) and will provide for delivery of hardware that is both consistent with the environments specified therein and consistent with the reliability class of the ACE payload.

This document gives design and test requirements and guidelines, rationale for those requirements, and suggestions for implementation. All **requirements are delineated in boldface type, numbered, and set off by double lines.** Recommendations are underlined. and *italics are used for emphasis.* The requirements stated here apply to all payload hardware. The Instrument Verification Matrix together with detailed procedures and test reports referenced by the Instrument Verification Matrix will describe how each instrument meets the requirements stated herein.

Environments addressed herein are: mechanical stress (both static and dynamic); thermal; electromagnetic; radiation; ground / shipping; and launch. An overview of observatory level test environments is also given.

1.2 Applicable and Related Documents

1) Payload Assurance Implementation Plan (ACE-CT-100-20)
Describes the practices used at Caltech to assure that instruments meet the reliability and lifetime requirements commensurate with the ACE mission objectives and in keeping with the product assurance requirements of the ACE Payload PAR (GSFC-410-ACE-008).

2) Spacecraft Environments Specification (APL-7345-9007)
Specifies the environments applicable to the ACE payload and recommends or requires certain tests be performed to assure compatibility with the S/C and with those specified environments. This is the primary source for information on observatory level testing.

3) Payload Verification Matrix (ACE-CT-100-024)
Specifies how instrument designers will meet the requirements outlined in this document, that is, what test or analysis procedures will be followed unresponsive to the environment design requirements.

4) Instrument Design and Data Packages (ACE-CT-XXX-42)
The IDDPs contain documentation of the test procedures and test results referenced in the verification matrix.

5) General Instrument Interface Specification (APL-7345-9005)
Specifies general interface requirements for accommodation on the spacecraft.

6) ACE Phase C/D proposal
Describes cost and schedule constraints on instrument development.

7) ACE Payload Management Plan (ACE-CT-100-030)
Describes management approach for the ACE payload thus dictating certain reporting and resource management requirements.

8) ACE Payload Configuration Management Plan (ACE-CT-100-031)
Describes Configuration Management Practices for the ACE hardware developers that apply to Caltech configured items and dictates that this document be under Caltech configuration management.

9) ACE Payload Resources (ACE-CT-100-40)
This document manages the resources of mass, power and data for the payload. All changes in these resources require a CR to this document.

1.3 Definitions

For purposes of this document the following definitions shall apply:

Assembly: a major functionally complete part of an instrument component (e.g. SOFT for CRIS, HVPS for SEPICA, Sensor Assembly for EPAM etc.)
Component: as viewed from the S/C, this is the major distinguishable part of an instrument (e.g. ULEIS Analog Electronics, MAG Electronics, SWEPAM-e, etc.) Some instrument consist of a single component (e.g. SIS)
Electronic Component: a component of an instrument which is entirely electronic and contains no detectors or external sensor elements (e.g. S3DPU or MAG Electronics box)
Ground operations: refers to any operation taking place prior to launch at any facility
Inherited Instrument: SWICS, MAG, EPAM, SWEPAM
Instrument: defined by the nine investigations on ACE (e.g. SWEPAM is considered one instrument with two components, SWEPAM-I & SWEPAM-E) The Observatory considers each instrument a "subsystem"
Instrument Test/Analysis Matrix: Matrix which cross-references each instrument, component, assembly and (sub-assembly) to a particular environmental design and test requirement. This replaces a verification plan and test plan which would normally be written.
Nominal operations: in-flight operations that encompass all planned activities. These would include all planned observatory operations, instrument calibrations, etc. but do not include contingency operations.
Observatory: the integrated S/C and payload
Part: an element of an instrument that is not subject to further subdivision e.g. a resistor, the hinge for a door, a bolt, a solid state detector, etc.

Protoflight: refers to a developmental unit which is readied for flight. A Prototype could become a protoflight if properly tested and qualified.
Prototype (brassboard): hardware that is built specifically for testing--usually is a faithful representation of what one expect to fly (without flight quality EEE parts for example.)
Qual test: a test used to qualify a design, procedure, packaging, or process.
Qual unit: an engineering unit built specifically for qual testing.
S/C=Spacecraft: That portion of the ACE Observatory built by APL--refers to all subsystems which support the flight of the instruments.
SEE=Single Event Effect: Includes upsets, latchup, burnout, gate rupture, or other events triggered by deposition of energy from a cosmic ray
Sensor Component: Component of an instrument that contains sensitive detectors, or electronics associated with them (e.g. ULEIS Telescope, SIS, MAG boom mounted sensors etc.)
Sub-Assembly: the next level below a functional assembly--usually refers to a circuit board, other examples would be the SOFT fiber planes, the SEPICA solid state detector, etc.)
Survival mode: mode referring to any off-nominal operation. In a thermal sense it always means that the instrument may be turned off.

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2.0 Environmental Verification Program

In accordance with the Caltech PAIP and GSFC PAR (Section 3.0), each instrument team will develop an Instrument Verification Matrix (test plan) which is summarized at the instrument component level in the Payload Verification Matrix. The Instrument Verification Matrix will couple each environmental design requirement to a particular test or analysis and *point to* both the test procedure (where a test is used) and report (generated as a result of a particular test or analysis). *Concurrence with this matrix /test plan by Caltech PMO constitutes approval of the flight qualification process. Successful completion of the tests/ analyses delineated in the Instrument Verification Matrix results in certification by Caltech that the Instrument or component has met the Environmental Design and Test Requirements of the ACE mission and should operate reliably in the environments specified by APL-7345-9007.* Figure 2-1 is a flowchart that illustrates the process that leads to certification of compliance with the requirements described herein.

Each instrument will have its compatibility with the ground, launch, and space environment verified and documented by taking the steps listed below.

R-2.1: An Instrument Verification Matrix & Test Plan listing the analyses and or tests performed in response to requirements stated in this document shall be developed.

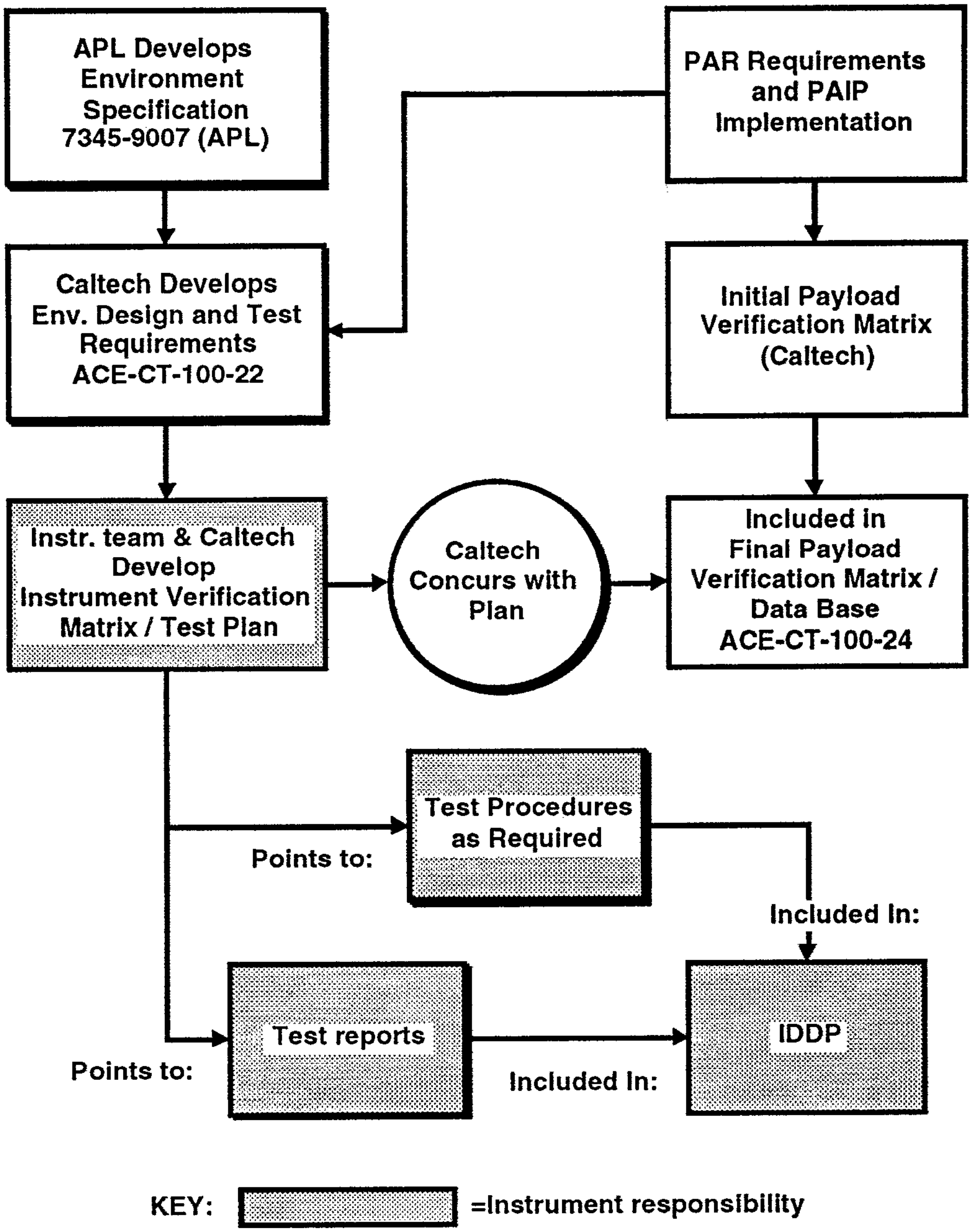
Caltech's concurrence with this plan and incorporation into the top level Payload Verification Matrix & Data Base (ACE-CT-100-24) constitutes approval of an Environmental Verification Plan for the instrument

R-2.2: Detailed procedures for each test of <u>flight</u> hardware shall be written and cross referenced to the test reports by the Instrument Verification Matrix. Those procedures shall be included in the IDDP.

<u>Reports describing any qualification tests performed on engineering units or assemblies as part of the development process should be included in the IDDP.</u>

R-2.3: A test report shall be prepared for each test performed on flight hardware, cross referenced in the Instrument Verification Matrix, and a copy included in the IDDP.

Figure 2.0-1 Environment Verification Flow



2.1 Test Documentation & Description

2.1.1 The Instrument Verification Matrix & Test Plan

This is a test plan which contains a detailed instrument verification matrix. The plan lists the tests to be performed, at what level the tests are performed, the test configuration (e.g. completed instrument or subassembly, etc.), and the test facilities. This plan will be developed by the Instrument Project Engineerin consultation with the Caltech Performance Assurance Manager and Caltech System Engineer.

A preliminary version of the verification matrix & test planshould be available at PDR and a final version at CDR. Inherited instruments should have a plan ready for review and comment at the time of their Inheritance Review.

2.1.2 Test Procedures & Reports

Test Procedures are prepared for any test involving flight hardware. These procedures should be peer reviewed by other members of the instrument team and by the engineer at the facility where the tests are performed. Test procedures can be designed so that key data are recorded right on the procedure form during the test. This allows very simple test reports and provides for easy trend analysis should certain tests be repeated several times. The test procedures are referenced in the Instrument Verification Matrix and should be included in the IDDP as a "bundled" deliverable for the pre-ship review.

Test reports will be written for all tests on flight hardware. Test reports on developmental items or engineering units are not required *unless they are part of the formal qualification plan.* Caltech encourages all developers to have a written record of all tests in a log book that is kept with the instrument. Test reports should be referenced by number (e.g. it might be an internal memo number) in the Instrument Verification Matrix. Test reports on flight hardware must include Caltech on distribution and should be affixed to the test procedure and included in the IDDP.

2.1.3 Instrument Functional Tests

It is important to thoroughly "ring-out" the instrument hardware before and after each environmental test to determine if there is any change in baseline performance. Recognizing that it is not always practical to test the sensor portion of an instrument after each environmental test because that may require operation in a vacuum as well as the use of an external stimulus (e.g. particle beam), it is still critically important that instrument teams develop some methodology to assess instrument health after each test so as to find any anomaly as early as possible.

R-2.4: As part of the test plan, each instrument team shall develop two functional test procedures for use during final protoflight qualification: a "comprehensive" functional used to characterize

the instruments state of health and performance (as completely as possible); and an "abbreviated" functional useful for quick checks at intermediate test stages. Results from these functional tests shall be recorded and included with test reports.

These procedures should become a "modular" part of all the instrument environmental test procedures. The standard test procedures are also needed by APL so they can be included in observatory test level procedures.

2.2 Qualification of New Designs

R-2.5: Instruments that are new designs shall use "protoflight" test levels.

Some new designs may use "qualification" levels for subsystem tests or development tests. (see Section 3.2 for an example.) It is important in the development of the Verification Matrix and Test Plan for a given instrument to *consider the design heritage* of the instrument, especially in cases where certain elements of that instrument, or certain packaging designs, piece parts etc. are being reused. *The Caltech Performance Assurance Manager will assist the Instrument Manager in these considerations during development of the Verification Matrix.*

2.3 Qualification of Inherited Hardware

Development of the Verification Matrix for inherited hardware must consider the test history of the specific component being selected for flight on the ACE S/C.

R-2.6: The instrument developer shall provide Caltech with as complete a history as possible of instrument qualification and verification tests on its previous program.

These include actual test plans, test reports, trend data, problem failure reports, in-flight performance, etc. The more information that is available about the instruments history the better Caltech can help tailor the Verification Matrix to the instrument and assure adequate qualification without overtest. In general, if inherited hardware has not been extensively modified, (extensive must be defined on a case by case basis) and previous test levels exceed the requirements of the ACE mission, the instrument may use the "acceptance" levels of the test specifications. In some special cases, retest may not be required.

2.4 Assembly Level Testing

Many times an instrument design has a particular assembly or sub-assembly that is problematic in a given environment. Caltech recommends that the instrument team work with the Performance Assurance Manager to develop a qual test program early in the development phase such that sensitivities of the particular subsystem can be isolated and the packaging designed to minimize those sensitivities at the component level.

R-2.7: Assembly level tests for developmental or prototype hardware, processes, or packaging techniques shall use "qual" test levels.

2.5 Margins

Margins are needed both in design and test to cover uncertainty in either the environment definition, the design or both. Caltech has reviewed each environment, is familiar with the margin philosophy and has tried to assure adequate margin without overtest when generating these design and test requirements. *Where an instrument has difficulty (because of conflicting design criteria) meeting an environment with the specified margin, both the margin, and the test philosophy will be reviewed.* Some tailoring of the requirements may be applicable. That tailoring will take place during the development and approval of the Instrument Verification Matrix & Test Plan.

2.6 Requalification Criteria

Once an instrument has completed its environmental test program or has been accepted for flight, and needs to be disassembled for rework or repair due to an anomaly or failure, Caltech will assess the applicability, the degree and the nature of any "requalification" testing. Caltech, together with the instrument provider will jointly adopt a plan that ensures the flight worthiness of the instrument and yet assures its reliability has not been compromised. Requirements for hardware acceptance by the APL integration team will still apply. (Refer to S/C GIIS)

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3.0 Mechanical Design and Test

The launch environment is the primary driver for the mechanical design and test criteria for the ACE Instruments. Structure borne vibration produced by the launch vehicle and conducted through the spacecraft, acoustically excited vibration, pyro-shock separation, as well as quasi static acceleration of the launch vehicle result in an cumulative force spectrum at the interface between the instrument and S/C. The instrument must be designed to accept this force, and subassemblies within the instrument must be designed to withstand the resulting accelerations. Designing an instrument to be compatible with this environment requires two different approaches depending on the frequency range of the expected accelerations.

At low frequencies, (less than about 80Hz) finite element analysis of the hardware coupled with the design case environment can be used to assure compatibility. For instrument components which have resonances well above the specified limits, all low frequency loads may be treated as quasi-static. (See Section 3.1) A sine dwell or sine burst vibration test may also be designed as part of the quasi-static loads verification. (This sine test would be distinct from that in section 3.2.1 .)

At high frequencies, qualification by analysis is not reliable so a two step approach which we shall refer to as "Design-to-Test" is followed: (See Section 3.2):

1) APL and Caltech first create a series of general test specifications which approximate and envelope the expected launch environment and include a specified margin for error. These test specifications are derived from specific launch environments for the hardware, that is the ACOUSTIC (air borne) and the RANDOM (structure borne).

2) Instrument developers then design their hardware to pass those tests. The instrument designer, together with Caltech, will develop a test plan that assures that the final flight hardware will survive the tests designed to simulate launch.

R-3.1: The instrument developer, and integrator, must assure that during the process of test, integration, shipping, or handling, the instrument is not subjected to loads or dynamic environments that exceed the design criteria.

Therefore this section shall also discuss the environments expected during observatory level testing. (Considerations for shipping and handling are given in Section 7.0).

This section is organized such that we shall discuss the low frequency and quasi-static environment first, followed by the high-frequency or vibroacoustic environment. In each case we shall identify the design and verification requirements as well as suggestions for implementation of the verification process.

3.1 The Quasi-Static Environment

R-3.2: A structure shall be designed to withstand its limit loads without experiencing yielding or failure.

The limit loads of a structure are the maximum physical loads that the structure will experience under all expected conditions of operation or use.

R-3.3: All structural design notes shall be retained in log books and are subject to review by the CIT ACE Payload Performance Assurance Manager.

Since finalized design loads depend on a coupling analysis between the S/C and the launch vehicle which is not yet complete, Caltech has selected to specify distinct qualification processes for new hardware vs. inherited hardware. Instrument design teams should refer to the appropriate section below.

3.1.1 Instrument Stiffness

Large amplitude transients induced by the launch vehicle coupled with resonance requirements on the S/C structure imply the need to assure that instrument components all have fundamental frequencies that are high enough so as not to be coupled to the S/C when excited by these events. This results in a "stiffness" requirement on each component. By meeting these stiffness requirements, instrument designers can treat the low frequency loads as quasi-static.

R-3.4: Instrument Components shall be designed such that their primary vibration resonances lie above 50 Hz for motion in the S/C x-y plane and above 70 Hz for motion along the S/C z axis (thrust axis). This requirement shall be verified by a low level sine survey. (See Section 3.2.1.1) For instruments mounted on brackets, this test shall be performed with the instrument component(s) mounted to the flight or "flight-like" bracket.

Although the overall instrument component may be shown to have a resonance well above these limits, it is important that component assemblies and sub-assemblies also meet the same requirement in order to assure no damage will result during the sine tests. The instrument test plan needs to describe how the sine sweep shall be instrumented to assure that the instrument component not only meets the minimum S/C requirement for resonances, but the instruments *internal assemblies* (in particular, the sensor assemblies) are not excited by transients associated with the sine or transient environments.

3.1.2 New Instrument Components

New instrument structural design may involve several steps. First, the structure undergoes its initial design. This design is detailed enough to enable finite element analysis. (Caltech can provide this analysis service upon request.) The design loads and safety factors used in this initial design (Figure 3.1-1 and Table 3.1-1) are based on a mass-acceleration curve for the delta II which envelope the actual loads experienced on a variety of spacecraft. By the time instruments have finished with this initial design process, the S/C and launch vehicle will have completed the coupled loads analysis and a loads specific to the ACE spacecraft will be available. The mass-acceleration curve that the instrument components have already been designed to (see Figure 3.1-1) will have enveloped these predicted loads. Should an instrument designer need to take some mass out of the structure or relax the design margin a bit, the new loads can then be used and incorporated into the design prior to CDR. Should the instrument not need to pull any mass out of the structure or redesign for other reasons, the preliminary design can stand because there is adequate margin built into the original curve presented here.

R-3.5: All new instrument components shall design their primary structure to withstand the limit loads given by the mass-acceleration curve in Figure 3.1-1 . Finite element analysis shall show that the initial design of the primary structure has safety margins indicated in Table 3.1-1 . These loads shall be applied separately in the three orthogonal axes to the component center of gravity. Add 2.2g to these loads for the thrust (z) axis.

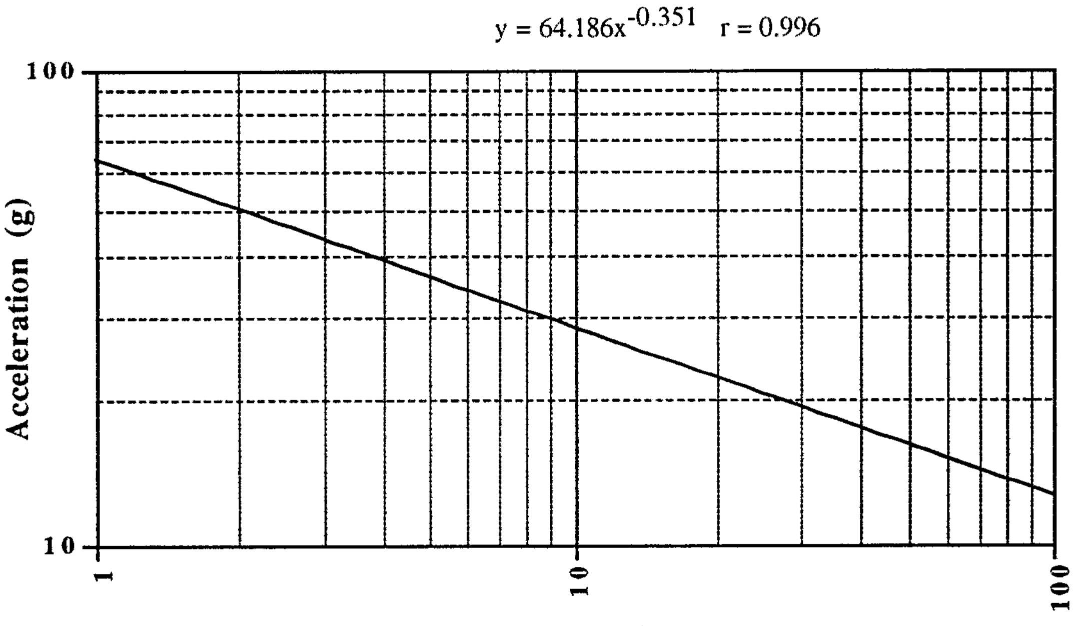
Note that if the instrument team elects to do a sine test (with a mass model to represent the secondary structures), a lower safety factor is required for the analysis.

Once the S/C coupled loads analysis is complete, specific loads will be available for top mounted vs. side mounted instruments and those instruments mounted with brackets will be distinguished from those directly mounted to the S/C structure. Designing to the curves in this document should assure compatibility with adequate margin and no need for redesign after the completed couple loads analysis.

Table 3.1-1 Design Load Factors

test factor	yield	ultimate
no test	1.6	2.25
1.25	1.4	1.8

Figure 3.1-1 Preliminary Mass-Acceleration Curve for the Delta II



3.1.3 Inherited Instruments (Including Build to Print)

Inherited instruments have already been designed and in most cases their structure has already been built. The purpose of the structural loads qualification process for these instruments is to assure that the environments of the ACE spacecraft and launch vehicle are compatible with the instrument's primary structural design. To this end, we will not compare the preliminary mass-acceleration curve to the instrument structural design but wait until the S/C to launch vehicle coupled loads analysis is complete.

R-3.6: The following information shall be provided to Caltech as part of the qualification process for all inherited instruments: 1) quasi-static loads applicable to the mission for which the instrument was originally designed; 2) the analysis or analysis/test program used to qualify the instrument for that mission; 3) the margins for yield and ultimate that exist for these given loads.

When the specific design loads for the ACE S/C are available Caltech and the instrument teams will assess the adequacy of the previous design and qualification process, determine if the current mission loads are enveloped by the previous loads and margins, and identify any actions which may need to be taken should the inherited design be judged inadequate for the expected loads on ACE.

3.2 Vibroacoustic

The vibroacoustic environment for the ACE payload has been derived by APL based on launch vehicle considerations, and spacecraft design. The test environments presented below (at the component level) represent the best approximation currently available of what will be experienced in flight.

R-3.7: Dynamics tests shall be performed at a facility and according to a test plan approved by Caltech.

Details of the test methodology such as the mounting fixture, or feedback control for shake tables, the size and baffling of acoustic chambers, etc. can be important variables in assuring that a given instrument component has an appropriate "simulation" of the flight environment.

R-3.8: Acceptance testing shall be for the indicated duration and at an amplitude 3dB below protoflight.

R-3.9: Protoflight level acceptance testing of the completed component or instrument shall be at the indicated levels and durations.

R-3.10: Qual testing of assemblies or subassemblies shall be at the indicated levels plus one additional minute duration beyond protoflight (in the case of a sine sweep this implies changing the rate).

3.2.1 Dynamic Test Environment

Instruments must be designed to ensure compatibility with the dynamics test environments described below. This includes a low frequency environment dominated by MECO/POGO events, engine ignition and other transients, a low frequency and lower intensity quasi-steady state and sinusoidal environment, a broadband random noise environment induced in the S/C structure by acoustic excitation, a direct acoustic field environment, and last of all, any shock induced by locally mounted electro-explosive devices. For each of the test environments described below the following requirements are applicable:

R-3.11: Test procedures shall be developed and test reports written as described in section 2.1.2 .

Test plans, (including selection of the facility and adjunct instrumentation) will be reviewed and approved by Caltech to help ensure against damage to flight equipment. *Should Caltech PMO not be convinced of a given lab's ability to provide for proper protection and handling of flight components, Caltech may elect an alternative lab* (cost deltas from the phase C/D contract will be negotiated with Caltech.) Each instrument's test plan will be tailored based on history, extent of sensitivity of critical components, degree of previous component qualification, and sensitivity to overtest. Caltech's Performance Assurance Manager, Systems Engineer and JPL support engineers will assist the instrument providers in developing a mutually acceptable plan.

R-3.12: A comprehensive functional test shall be conducted prior to and after the 3 axes of vibration testing have been completed. At least an "abbreviated functional test" shall be conducted after each axis.

Completion of the instrument level Verification Matrix simply involves a reference to that appropriate test report. Test reports for more than one test may be combined if appropriate.

R-3.13: For instruments mounted on brackets, these tests shall be performed with the instrument component(s) mounted to a flight or "flight-like" bracket.

R-3.14: All newly designed and/or newly constructed instruments shall use protoflight levels if qual testing has not been done. Inherited instruments shall indicate test levels and durations in the instrument test plan for concurrence by Caltech.

3.2.1.1 Sine Survey

R-3.15: Prior to any other dynamics testing, a sine survey shall be performed from 5 to 2000 Hz at a level of 0.25 g to identify all major resonances of each instrument component and verify the stiffness requirement. An additional survey shall be used after dynamics testing to verify that no degradation has occurred.

3.2.1.2 Sinusoidal Vibration

That part of the launch vehicle environment which is sinusoidal in nature and *quasi-steady* in its input is best approximated by the sine vibration test. Our sine environment has also been designed to simulate flight transients induced by launch vehicle events such as MECO, POGO, second stage ignition etc. These environments have taken into consideration the coupling between the S/C structure and the launch vehicle, and have also considered the specific instrument mounting locations.

R-3.16: Protoflight instrument components shall survive without degradation a three axes test at the levels illustrated in applicable Table 3.2-1 through Table 3.2-3 . The sine test shall consist of one upsweep at 4 octaves/minute in each of three orthogonal axes at the indicated levels with an accuracy of ±10%. The method of limiting the component response levels during this test so the maximum expected levels predicted by the ACE/Delta II coupling analysis are not exceeded shall be specified in the test plan.

(Results of the coupling analysis are not available at the time of release of this document.) Level and duration of the sine test for inherited instruments will depend on their test history and the degree of modification for ACE. Nominally, an "acceptance test" which is 3db below that for protoflight would be expected.

Table 3.2-1 Protoflight Level Sine Test A
(applicable to ULEIS analog electronics, MAG MFI, and S3DPU)

Thrust Axis (z)		Lateral Axes	
Frequency (Hz)	**Acceleration (zero to peak)**	**Frequency (Hz)**	**Acceleration (zero to peak)**
5-6.2	.5 inch (peak to peak)	5-6.2	.5 inch (peak to peak)
6.2-50	1.0g	6.2-15	1.0g
50-60	14.0g	15-20	7.5g
60-100	1.0g	20-100	1.0g

Table 3.2-2 Protoflight Level Sine Test B
(applicable to SIS, ULEIS telescope, ULEIS DPU, SEPICA, SWICS, EPAM, SWEPAM I & E)

Thrust Axis (z)		Lateral Axes	
Frequency (Hz)	Acceleration (zero to peak)	Frequency (Hz)	Acceleration (zero to peak)
5-6.2	.5 inch (peak to peak)	5-6.2	.5 inch (peak to peak)
6.2-20	1.0g	6.2-15	1.0g
20-25	14.0g	15-20	7.5g
25-38	1.0g	20-100	1.0g
38-48	7.0g		
48-100	1.0g		

Table 3.2-3 Protoflight Level Sine Test C
(applicable to CRIS, SWIMS, MAG sensors

Thrust Axis (z)		Lateral Axes	
Frequency (Hz)	Acceleration (zero to peak)	Frequency (Hz)	Acceleration (zero to peak)
5-6.2	.5 inch (peak to peak)	5-6.2	.5 inch (peak to peak)
6.2-20	1.0g	6.2-60	1.0g
20-25	14.0g	60-80	2.0g
25-100	1.0g	80-100	7.5g

3.2.1.3 Random Vibration

The random vibration environment results from a combination of vibration transmitted mechanically through the base of the spacecraft, and acoustically excited vibration of the spacecraft honeycomb panels (to which the instruments are mounted).

R-3.17: Protoflight instrument components must survive the random vibration test spectrum and duration as given in Table 3.2-4 . The spectral shape shall be within ±3dB and the overall level shall be accurate to ±1.5 dB

Level and duration of the random test for inherited instruments will depend on their test history and the degree of modification for ACE.

The spectral values given in Table 3.2-4 are inputs at the instrument mounting points. The test must be conducted in each of three orthogonal axes, one of which is parallel to the thrust axis. *The instrument team needs to carefully consider a vibration test method which can protect against the overtest that results from differences between the relatively compliant S/C structure and the "infinite impedance" shake table.* Caltech recommends the use of force-limiting during this test. A more traditional alternative, the practice on notching the input spectrum to limit the component response, is acceptable when data from the S/C structure dynamics test is properly utilized, and the test is properly designed. In either case both Caltech and APL must participate in the development of the test procedure to assure that force limiting or notching, as it is applied, is consistent with the modeled/measured S/C responses.

R-3.18: The Instrument Test Plan shall describe the method and facility used to assure against overtest.

An additional concern during all vibration testing is the perming of soft magnetic materials due to uncompensated or poorly compensated shaker coils. Caltech will work closely with the instrument teams to help assure minimum exposure to stray fields and the MAG team will be involed if any "sniffing" or deperming activity is deemed advisable.

Table 3.2-4 Protoflight Level Random Vibration Test Level
Overall Amplitude = 14.8g RMS; Duration = 1 minute.

Frequency (Hz)	Power Spectral Density (g^2/Hz)
20	0.02
20-100	+3.4dB/Oct
100-300	0.12
300-400	+3dB/Oct
400-830	0.16
830-2000	-3dB/Oct
2000	0.066

3.2.1.4 Acoustic

The acoustic environment is determined by the launch vehicle, the faring size, position of the S/C within the fairing, and acoustic blanketing. Not all instrument components or their assemblies are affected equally by the flight acoustic environment. The sensitivity to acoustic fields and thus the need for an acoustic test should be evaluated based on surface mass density and surface area. This is best accomplished by analysis which Caltech can provide upon request. The integrated observatory will undergo a "protoflight" level acoustic test. (See Section 3.4) *It is critical that instrument components not discover failures at this late date.*

R-3.19: The instrument test plan shall describe how the instrument design will be compatible with this acoustic environment.

Caltech recognizes that acoustic testing can be expensive and there are few facilities qualified to give a realistic and reliable test. *For those instruments which identify components or assemblies that may be sensitive to the acoustic field and thus elect to do a qualification test, Caltech will provide assistance in selecting a test lab, monitoring the test, and in dealing with subsequent problems should they develop.*

The protoflight acoustic test environment consists of a reverberant acoustic field with levels and on-third octave center frequencies given in Table 3.2-5 . The Spectrum of the test yields an OASPL of 147.6 dB. (0dB=2×10^{-4} dynes/cm^2 or 20 μPa) Duration of this test shall be 1 minute. Assemblies within instrument housings may not need to be qualified to these levels because the housing itself provides for some attenuation. Caltech can support the analysis required to determine the proper test level and shielding provided by the structure if requested.

Table 3.2-5 Protoflight Acoustic Test Level

Center Freq. (1/3 Oct.) Hz	Sound Pressure Level (dB)
31.5	123.5
40	125
50	126.5
63	128
80	130
100	131
125	132.5
160	133.5
200	134.5
250	135.5
315	137.5
400	139
500	141
630	138
800	135
1000	133
1250	131.5
1600	130.5
2000	129.5
2500	128.5
3150	127
4000	125.5
5000	124.5
6300	123.5
8000	122.5
10000	121.5

3.2.1.5 Shock

The shock introduced by payload separation does not require any special tests for instrument qualification. The spectrum and levels at the instrument mounting locations is well enveloped by the previously described tests. However, instruments which employ pyrotechnic devices should include as part of their test plan a method to assure that those devices do not impact the survival or functionality of any part of the instrument component.

3.2.2 The "Design-to-test" Methodology

A "design-to-test" methodology must be used in cases where no reasonable analytical approach exists. *Design-to-test does not mean that an instrument is simply designed, then, when completed, it is tested to qualify for flight.* This process could only work (with a low risk to schedule and cost) for instrument designs which have *previously been qualified to identical or greater levels. Design-to-test means that the design process must include some methodology to assure that the instrument meets the required test environment.* The final test simply acts as proof that the methodology has been sound. "Design-to-test" must apply to the vibroacoustic environment described above.

Designing to these test environments depends on heritage--even for new instruments. It depends on heritage of:

1) piece parts

2) materials

3) processes

4) packaging

Caltech will assist the instrument developers in each of the above areas. Piece parts will be reviewed with an eye on a number of criteria which will include (for certain classes of parts) their vibroacoustic sensitivity. Likewise, submittal of a materials list will identify materials which may be problematic in this arena. Processes relevant to vibroacoustic design compatibility include material usage, assembly procedures, fastener usage etc.

Packaging design is probably the key element of the design-to-test method. There are numerous do's and don'ts that have been assembled into packaging guideline documents which are available at any instrument developers request from Caltech. Instead of requiring that everyone "design to" these documents, Caltech will be using a packaging expert to review an instrument's packaging design and provide recommendations and suggestions for improvement.

R-3.20: Prior to CDR and the beginning of fabrication, instrument developers shall provide enough detail on the packaging design and fabrication processes to allow a detailed packaging / manufacturing assessment by Caltech.

The assessment will most likely be carried out at the developer's institution and will be informal in nature. *Status of the packaging design will be a key element of the CDR agenda.*

One area where corporate knowledge can be of little assistance is that of sensor design, mounting, and packaging. *Instrument providers need to think carefully about how the sensor will be qualified to the vibroacoustic environment and document that process in their test plan.* Instrument developers should consider a step by step process for sensor development consisting of engineering models coupled with qualification testing. A sensor qualification plan will be very different for the various ACE payload components because of their varying sensitivities to the vibroacoustic environment, therefore Caltech shall review this particular element of the test plans on a case-by-case basis. A preliminary version of the sensor test plan needs to be available by PDR.

3.3 Instrument Cavity Pressure Changes

Relief ports on instrument cavities must be designed to accommodate the maximum pressure change associated with ascent after launch (1 psi/s).

R-3.21: Component relief ports that exceed 5E-4 in^2 area per in^3 of volume shall require no further analysis to meet the pressure change compatibility requirement.

Instruments sensitive to acoustic fields should consider the effect of the relief port on acoustic shielding. Caltech will provide assistance with this analysis when requested.

3.4 Observatory Level Tests

Observatory level testing is described in detail in the APL Environmental Specification 7345-9007. This section gives an abbreviated description enabling the instrument designers to make comparisons to component level test requirements described herein.

Observatory level dynamics testing begins with a sine survey which will be performed from 5 to 2000Hz at an acceleration of 0.25g (rate = 4 octaves/minute).

The next step will be to perform a sinusoidal vibration test. The levels of this test are summarized in Table 3.4-1 and are the inputs at the S/C to launch vehicle interface. Response will be limited to assure that the design load levels predicted are not exceeded.

Table 3.4-1 Observatory Level Sine Test

Thrust Axis (z)		Lateral Axes	
Frequency (Hz)	Acceleration (zero to peak)	Frequency (Hz)	Acceleration (zero to peak)
5-6.2	.5 inch (peak to peak)		
6.2-100	1.0g	5-100	0.7g

The level of the full-up observatory random vibration is illustrated in Table 3.4-2 . The overall level of this test is 8.5 g RMS and will have a duration of 1 minute for each of 3 orthogonal axes. All hardware that has been certified through the payload environmental qualification program should experience no difficulty with this test. Previously conducted sine surveys will be used to assure that there is no overtest at resonant frequencies.

Table 3.4-2 Observatory Level Random Vibration Test
Overall amplitude = 8.5 g RMS; Duration = 1 minute

Frequency (Hz)	Power Spectral Density (g^2/Hz)
20-100	0.002
100-300	+9.3dB/Oct
300-700	0.06
700-2000	-3dB/Oct
2000	0.021

Once integrated, the whole observatory (with thermal blankets installed) will undergo a "protoflight" level acoustics test. *This test exposes the components to the maximum expected flight levels plus 3 dB*. The Spectrum of the test yields 147.6dB. (0dB=$2x10^{-4}$ dynes/

cm^2) Duration of this test will be 1 minute. The 1/3 octave band sound pressure levels are given in Table 3.2-5 .

3.5 Mass Properties

Mass properties do not constitute an environment as such, however, accurate mass properties of instruments are critical for S/C balance, important for accurate coupled loads analysis, and in necessary to ensure that the S/C principal axes are lined up with the geometrical axes. Accurate mass properties are also important in the assessment of the "force spectrum" for instruments that implement force limited vibration tests. Caltech maintains configuration management of all payload mass estimates in "Payload Resources" ACE-CT-100-40. Changes in mass estimates must be submitted to Caltech by a CR to that document.

The knowledge of the instrument mass properties improves with time so the following goals have been set and are given in Table 3.5-1 . *Inherited instruments will have these goals for CDR apply at their inheritance review.*

Table 3.5-1 Mass Properties

Mass property	PDR	CDR	Delivery (pre-ship review)
Mass	allocation	10%	1% or 100g whichever is less
Center of Gravity	N/A	10%	0.5cm
moments of inertia	N/A	10%	10%

4.0 Thermal Design and Verification

Good thermal design is a key element towards assuring a smooth test phase at the observatory level. It is also key to assuring long instrument life and reliable operation.

The following sections describe the thermal design and test methodology Caltech prescribes for all the instruments. New instruments will "start from scratch" determining their sources and sinks, operational constraints, thermal control methodology, and detailed thermal design. Inherited instruments have the specialized problem of determining whether their existing thermal design is compatible with the ACE spacecraft and mission profile. Inherited instruments should address all of the requirements and tests described below in their test plan and inheritance review. Caltech will work with each team individually to determine which tests need to be done and how they could best be done. Both Caltech and APL are available to help assist instrument teams in their thermal engineering.

4.1 Design Requirements

Instrument component thermal design and verification has four principal elements:

1) Establish temperature limits associated with the in-spec operation and survival of critical sensor elements, electrical and electromechanical components;

2) Establish and characterize the external environment sources and sinks;

3) Execute the detailed thermal design to assure operation of critical elements over the entire range of environmental inputs within constraints established in (1) and with margin specified in section 4.2;

4) Produce a test plan, generate detailed test procedures, and conduct the testing that will serve to validate the design;

In this section we shall detail those requirements and recommendations associated with this design process.

4.1.1 Temperature Definitions & Limits

R-4.1: For purposes of thermal analysis and test, each sensor component shall have the AFT and survival temperature ranges as well as minimum operational temperatures specified for all *key* assemblies or sub-assemblies.

These ranges are defined as follows:

Allowable Flight Operational (or "in-spec") Temperature (AFT): the temperature range over which the instrument element can be allowed to operate in flight. This is the range over which the instrument assembly will be calibrated and operate within specification.

Survival range: the temperature range over which the assembly or part may be exposed (in a non-operating mode) without suffering any permanent degradation. The survival range for an entire instrument component may be dictated by the most sensitive element of that component and how effectively the thermal design is balanced.

The minimum turn-on temperature for any ACE payload assembly or subassembly will be the minimum temperature at which it can be operated. (It must also be ground tested to this temperature.)

The ACE S/C will not have "warm-up" heaters which would be activated *in addition to* the normal survival heaters prior to applying power to the instrument component. Thus the minimum turn-on temperature (which is likely to be much higher than the actual survival temperature) is really what dictates the on-orbit design constraint for the "survival" heater (see section 4.3.2).

Instrument components consisting only of non-temperature critical electronics (that is components which do not have their temperature limits set by any sensitive sensor assemblies or electromechanical devices) shall have the above temperature ranges defined as follows:

R-4.2: Instrument electronic components and individual electronics sub-assemblies such as circuit boards shall have an AFT range of -23°C to +55°C (defined at their primary thermal interface with the spacecraft); survival temperature shall be specified on a case by case basis; and minimum turn-on temperature shall be -28°C.

In addition to these on-orbit temperature constraints, the instrument thermal engineer should work with the instrument team and Caltech to define clearly the *operational and non-operational test temperatures* of all instrument hardware keeping the test margin requirements in mind (see section 4.2). For an illustration of the relationship between AFT, survival, predicted, and test temperatures, see Figure 4.2-1

4.1.2 Instrument Thermal Coupling to S/C

Those instrument components that are mounted to the S/C may be either conductively coupled or thermally isolated. When conductively coupled, a thermal design may utilize either primarily conductive paths for thermal control or a combination of conductive and radiative. Instrument components which use only the conductive path for thermal control need to consider the interface temperatures defined in Table 4.1-1 .

Those instrument components that are not conductively tied to the S/C must use their own surfaces for control via radiation.

R-4.3: Instruments not conductively tied to the S/C shall utilize a thermal design which minimizes thermal sensitivity to the S/C environment (S/C or other instrument surfaces & temperatures).

That is, their thermal balance should depend only on the angle of the instrument with respect to the sun, and on their internal heat generation. Blankets need to be designed to assure that the instrument thermal control can "stand alone" and that verification of that control can be achieved at the component level prior to observatory testing. Careful consideration of other "sneak paths" such as deck or adjacent instrument radiation, and harness or cable conduction is particularly important in this case.

4.1.3 Environments

R-4.4: Instruments shall design to the interface temperatures under operational and survival conditions defined in Table 4.1-1 .

The solar input should be defined by considering that the angle between the S/C +z axis and the sun can vary between 0° and 20°. APL can provide each instrument with a model of the solar input and help determine view factors for instrument radiators if requested. The launch phase will have heater power available to instruments so that they can be assured of being above their minimum turn-on temperature.

Table 4.1-1 S/C Interface Design Temperatures

Component type	Nominal mode temperatures (Celsius)	Survival mode temperatures (Celsius)
Sensor component tied to deck	-15 to +15	-25 to +15
Electronics component tied to deck	-23 to +55	-23 to +55
Component thermally isolated from S/C	-20 to +40 top -10 to +40 side	-25 to +40 top -10 to +40 side

4.1.4 Design

Given the thermal environments (sources and sinks) and the temperature ranges of the instrument component(s), the job of the thermal engineer together with the mechanical, and packaging engineer is to provide a thermal design that meets the following requirements:

R-4.5: Under worst case flight conditions, (including beginning of life and end of life extremes for surface absorptivity and emissivity) and for the environments specified in Table 4.1-1, the thermal analysis shall predict that *all instrument assemblies* are maintained at least Δt_0 inside their specified AFT (Δt_0 is defined in Table 4.2-1).

R-4.6: In the case of *contingency* operations or other periods where the instrument has been turned off, the thermal analysis/design shall assure that *all assemblies* are maintained above their minimum turn-on temperature with a margin Δt_s (Δt_s is specified in Table 4.2-1)

Figure 4.2-1 illustrates the relationship between the AFT, the minimum turn-on temperatures, and the two specific thermal design requirements listed above.
In addition to critical sensor elements, it is important that the designer assure that electronic parts are also operating within allowable limits.

R-4.7: At no time during ground testing shall electronic part junction temperatures be permitted to exceed 110°C or that specified by the manufacturer (and suitably derated) whichever is less. Likewise, with exception of short duration excursions, thermal design shall assure junction temperatures in flight shall be held to less than 70°C.

As an example of how to respond to this requirement, consider designing circuit boards for a maximum rise of 35°C between the junction and the reference surface (that would be the baseplate for conductively mounted components). This allows testing to a baseplate temperature of 70°C (to meet the testing requirements described later in this section) yet gives a 5°C analysis margin under the 110°C limit set by the above requirement.

Determination of junction temperatures is especially important with power supply boards, boards that contain electronic parts which dissipate more than 40mw (as a rule of thumb), or boards with high packaging density. *Every 25°C reduction achieved on in-flight junction temperatures achieves about an order of magnitude increase in part life.* Instrument teams should consider the use of CAD tools which allow the calculation of thermal paths during circuit board layout. As an alternative to a detailed analysis of those parts suspected of being under thermal stress, thermographic mapping of brassboard or engineering prototype boards should be used if time is allowed to correct for defects uncovered by the test. Caltech can provide support for such analyses or test where required.

R-4.8: Instrument thermal design shall be compatible with all test requirements and margins described in this section.

R-4.9: The thermal design of an instrument must be verified by test (independently of the spacecraft).

4.2 Design and Test Margin

Margin in the thermal design process allows for uncertainty in thermal modeling, and margin in the test phase adds further confidence in the final product and provides for additional reliability by assuring that actual operation on-orbit occurs well within the extremes of the hardware capability. Margin during the early phase of the design process is particularly important because there are uncertainties associated with the packaging of the electronics and sensors elements which preclude highly accurate and reliable temperature predictions at the locations where temperatures may be critical.

R-4.10: Instrument thermal design shall consider the analysis and test margins described in Table 4.2-1 .

Figure 4.2-1 illustrates the relationship between the specified temperatures (AFT, survival, and minimum turn-on) and the design and test margins specified in the Table 4.2-1 . *It is important to understand that these margins represent good design rules. In any particular case, the design and test margin may have to be traded or the total margin may need to be either greater or less than specified in order to accommodate special test or operational constraints, reliability or design life concerns, or practical limitations of the thermal design and resource availability. Lead engineers need to work closely with Caltech and the thermal engineer in reaching a consensus on the right margin to apply at any specific stage of analysis or test. These margins must be clearly stated in or referenced by the test matrix.*

Table 4.2-1 Thermal Design & Test Margins

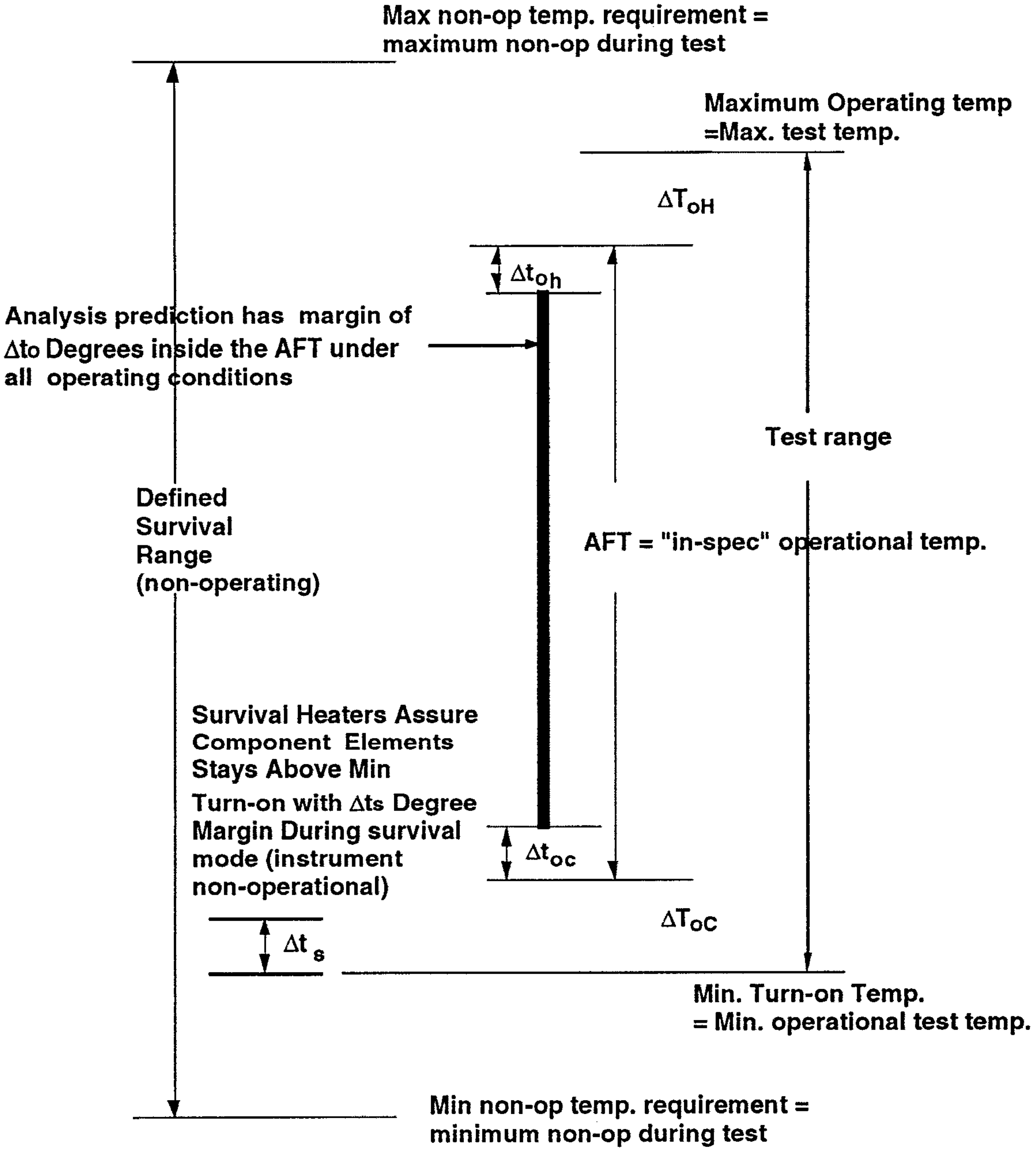
Component Type		Design case deck interface temp	Component AFT or "in-spec" temp.	Analysis Margin (Δt_o & Δt_s)	Test Margin (ΔT_{oH} & ΔT_{oC})
Sensor Tied to Deck	operate	-15° to +15° (Operate)	Specify AFT ("in-spec") at key assemblies	$\Delta t_{oh} = 5°$ Δt_{oc} = 10° passive 5° active** (at defined locations)	$\Delta T_{oH} \geq 10°$ $\Delta T_{oC} \geq 5°$ (at defined locations)
	survive	-25° to +15° (Survive)	Specify min & max non-op temp at key locations plus min turn-on	Δt_s = 10° passive 5° active* (at defined locations)	Test to specified non-op during t-vac
Sensor Isolated from Deck or S/C	operate	-20° to +40° (top mounted) -10° to +40° (side mounted)	Specify AFT ("in-spec") at key assemblies	$\Delta t_{oh} = 10°$ Δt_{oc} = 10° passive 5° active** (at defined locations)	$\Delta T_{oH} \geq 15°$ $\Delta T_{oC} \geq 10°$ (at defined locations)
	survive	-25° to +40° (top mounted) -10° to +40° (side mounted)	Specify min & max non-op temp at key locations plus min turn-on	Δt_s = 10° passive 5° active* (at defined locations)	Test to specified non-op during t-vac

Table 4.2-1 Thermal Design & Test Margins

Component Type		Design case deck interface temp	Component AFT or "in-spec" temp.	Analysis Margin (Δt_o & Δt_s)	Test Margin (ΔT_{oH} & ΔT_{oC})
Electronics Tied to Deck	operate	-23° to +55°	AFT= -23° to +55° (at baseplate)	$\Delta t_{oh} = 10°$ $\Delta t_{oc} =$ 10° passive 5° active** (on predicts for deck temp)	$\Delta T_{oH} \geq 15$ $\Delta T_{oC} \geq 5°$ (at baseplate)
	survive	-23 to +55	to be defined for each component (-40 to +85 typical)	$\Delta t_s =$ 10° passive 5° active* (on predicts for deck temp)	Test to specified non-op during t-vac

* Implies use of "survival" heater
** Implies use of "operational" heater(s)

Figure 4.2-1 Thermal Analysis and Test Methodology



4.3 Thermal Monitoring & Control Hardware

Varying strategies may be employed by the instrument designer for thermal control. These are usually dictated by the operational limits of specific sensors within the instrument, whether or not the instrument component is tied to the deck, the deck interface temperature, etc. Instrument teams should be aware of the following requirements and recommendations related to the selection and placement of thermal sensors and the use and control of heaters.

4.3.1 Sensors

Instrument health cannot be adequately monitored during flight without proper placement of thermal sensors.

R-4.11: Instrument designs shall assure that thermal sensors conditioned by the S/C are placed so as to verify the allowed operational and survival temperature limits on each component's critical assemblies. The location of all S/C powered temperature sensors shall be specified in the SIIS thermal interface drawing.

Likewise, ground tests cannot verify the component's thermal design/performance and the thermal analysis unless the an adequate number of thermal sensors are provided and those sensors are properly located within the component.

R-4.12: Designers shall assure that the instrument thermal design provides adequate internally mounted thermal sensors to assess thermal design/performance and to monitor key assemblies during instrument level tests.

(Some of these "test monitoring" thermistors may be conditioned and read out though a test connector by the instrument GSE).

4.3.2 Heaters

The instrument designer must determine the need for "operational" heaters (heaters contained within the electronic box for equalization of temperatures under normal operational conditions) and also whether the instrument needs "survival" heaters.

In cases where different instrument sensor assemblies have widely differing operational limits, it may be necessary to include operational heaters in the design to achieve acceptable temperatures. Operational heater power is budgeted to the instrument and any *changes in the estimated heater power or resizing or heaters requres a CR (Change Request) to the power resource allocation table managed by Caltech..*

Survival heaters are used to make sure that an instrument component's key assemblies and subassemblies stay above their minimum turn-on temperature during powered-off periods. Survival heater power is included in the S/C power budget.

R-4.13: Survival heaters (when used) shall keep the instrument's critical assemblies at the minimum turn-on temperature (with a margin described in Table 4.2-1).

To save power, consideration should be given to placing these survival heaters as close as possible to the most sensitive element (inside the instrument component if possible).

R-4.14: The size (power consumption), type, location and thermostat setting of all operational and survival heaters shall be documented in the SIIS thermal interface drawing.

4.4 Test Requirements

An appropriate set of thermal tests needs to be conducted to accomplish the following objectives:

1) demonstrate the performance (with margin) of each component over a range of temperature beyond what is expected in flight (compatibility of a components electrical and sensor design with the thermal environment);

2) demonstrate that all components of an instrument, which must function together in flight, do so satisfactorily over a temperature range beyond what is expected in flight;

3) verify the compatibility of the thermal design with the expected environment (capability of the design to maintain temperatures within specified limits);

4) assure that the quality of workmanship (selection of materials, use of processes etc.) is such that it will withstand the rigor of the system test, launch, and flight environments;

5) uncover any incipient problems and infant mortality associated with electronic and/or electromechanical parts and assembly processes.

In order to achieve the above objectives each instrument component shall undergo a test program that incorporates the following elements:

a) Voltage margin test

b) Thermal cycle (optional)

c) Thermal soak

d) Thermal vac

e) Thermal balance

Details of these five elements are described in the following paragraphs.

4.4.1 Voltage margin test

The voltage margin test is a reliable replacement for worst case analysis when implemented at the board or subassembly level and supports test objective number one above. The purpose of the test is to verify the "robustness" of the design, that is that no circuits are on the "edge" and operating only marginally at the beginning of life. All new boards and subassemblies should be subjected to a voltage margin test described as follows:

a) the test shall be carried out at the upper and lower qual temperatures (+70°C and -25°C) in a non-vacuum environment;
b) each element under test shall be powered from a regulated supply that has the ability to vary the voltage (on the order or 1% accuracy is advised);
c) the element shall then be tested at both temperature extremes at the nominal and plus and minus 7% of nominal supply voltage.
d) In spec operation should be verified in all cases.

A good test at this level can alleviate many problems at later and higher levels of assembly.

R-4.15: Each test plan shall state assemblies on which the voltage margin test will be performed.

4.4.2 Non-Vacuum Thermal Cycle

The thermal cycle test is designed to assist in the accomplishment of objective 4 above. That is, to verify that the materials, parts, and processes used in constructing a subassembly or assembly are sound and without any incipient flaws. In a program such as ACE where thermal cycles are not expected on orbit, the thermal cycle test should be primarily used as a *process qualification test* for any new or complex assemblies that are designed from materials with differing thermal properties. *This is not considered a protoflight test for ACE hardware because little or no thermal cycling will take place after launch.* The thermal vac soak test should be used instead to find incipient failures of protoflight components.

The level of assembly at which thermal cycling tests are completed depends on variables like the similarity of subassemblies, the ease of test, the ability to monitor performance, and the compatibility of the subassemblies in terms of their temperature limits. In general, assemblies should be tested as functional units. *This test is not required by Caltech for protoflight electronic assemblies and will be discouraged for completed and inherited hardware which have already undergone environmental acceptance testing.*

R-4.16: The instrument developer shall identify the assemblies and subassemblies to be thermal cycle tested in the test matrix. The temperature limits of the thermal cycle test and the number of cycles shall also be noted in the test plan.

Consider this test for all **sensor** assemblies at the **engineering prototype level.** It is critical to note limitations on testing imposed by certain materials, coatings etc. For example, solithane has a glass transition temperature ranging from -3°C to -22°C (depending on formulation) with a typical value of about -5° but most stress is induced below -20°C.

The thermal fatigue life of a packaging design must be robust enough such that the manufacturing, test, and integration process consumes less that 5% of the toal available fatigue life. Inherited instuments should provide as complete a history of the hardware as possible, including processing, manufacturing, and testing thermal extremes and number of cycles. For example, log books that indicate the total number of turn-ons is useful in Caltech's evaluation.

If the instrument designer elects to cycle individual flight electronic assemblies (rather than using the cycle test as a *process qualification* mechanism, The number of cycles should be ≤ 10 for a ΔT of 50°C and the rate of change of temperature should be at $<$2°C/ minute. The subassembly or assembly should be monitored continuously during the test with selected parameters recorded automatically at regular intervals.

R-4.17: Results of thermal cycle tests (when performed on flight hardware) shall be recorded in logbooks, and any anomalies dealt with according to the configuration management and anomaly reporting system as described in the Caltech Configuration Management Plan and applicabe IAIP. The last three cycles shall be failure free. Any rework after the test must be documented consistent with the CIT approved configuration management practices. The need for any re-test after rework shall be determined by procedures consistent with the PAIP.

4.4.3 Component or Assembly Level Thermal Vac Soak

The thermal soak test is designed to be both a "burn-in" test for the *electronic assemblies* (objective 4 & 5 above) at hot temperature and an operational test at cold extremes. *It is probably the most critical test for helping to assure a long life once in* *space.*

R-4.18: All flight electronic subassemblies and printed circuit boards shall undergo a thermal vac soak. The hot test shall be performed at a temperature of +70°C (15° above AFT for electronic assemblies) in a thermal vac chamber for a duration of ≥144hr. The cold test shall be at a temperature of -25°C for a duration of ≥ 24 hours. Electronics shall be on at all times and key housekeeping and performance parameters should be recorded for trends.

This test can be accomplished at the board level or at the assembly or component level (where it could be part of the normal thermal vac testing). Because of time and resource constraints, *it is recommended that this test be conducted at the highest level of assembly that is practical* (e.g. prior to installation of detectors or other elements which may preclude the necessary thermal excursion). The operational time accumulated during this test may be counted toward the 240 hr error free operation requirement prior to instrument delivery *if the test is performed at a sufficiently complete level of component integration.* For cases where it is impractical to do this test in a vacuum, it may be performed in air at a suitably higher temperature (15°C typ.).

4.4.4 Instrument Level Thermal Vac

The instrument level thermal vac test addresses the first two objectives of our test program, namely to assure that the instrument component(s) operate in an environment beyond what is expected during flight and that they operate together (for multiple component instruments). Some thermal model verification (objective 3) is possible for well-designed tests. In addition, the thermal vac test, as proposed below, is an opportunity to do a pseudo "bake out" of all instrument components and interconnecting cables prior to delivery. The profile of the suggested test uses the first segment of the TV test for reducing the level of contamination and improving the quality of the vacuum.

R-4.19: A thermal vac test shall be performed on the complete instrument (including all components) as the *final step* in the thermal testing process. The test shall consist of at least 3 cycles with a duration of at least 96 hours. All mechanisms will be exercised at each operational temperature extreme and at least one "cold start" and one "hot start" are required.

A number of parameters characterize the thermal vac test, namely, the upper and lower limits, the transition rates, the number of cycles, and the operational scenario. The following definitions apply: (Definitions of ΔT_{oH} and ΔT_{oC} are given in Table 4.2-1)

upper operational test limit: Maximum AFT for the components $+\Delta T_{oH}$

lower operational test limit (equal to minimum turn-on temperature): Minimum AFT for the components $-\Delta T_{oC}$

upper non-operational test limit: Maximum survival temperature;

lower non-operational test limit: Minimum survival temperature;

transition rate: T-vac transition rates should not exceed the maximum allowable transition rate for the most sensitive assembly (determined by the design team) or 30°C/hr. whichever is less;
number of cycles: A cycle is defined as transition from one extreme to another and back again (note at least 3 are required);
operational scenario: Specifies when and for how long the instrument will be operated (Figure 4.4-1 illustrates a typical thermal vac temperature and operational profile consistent with the requirements specified herein);
Duration: Total duration of instrument operation during the test (at least 96 hours).

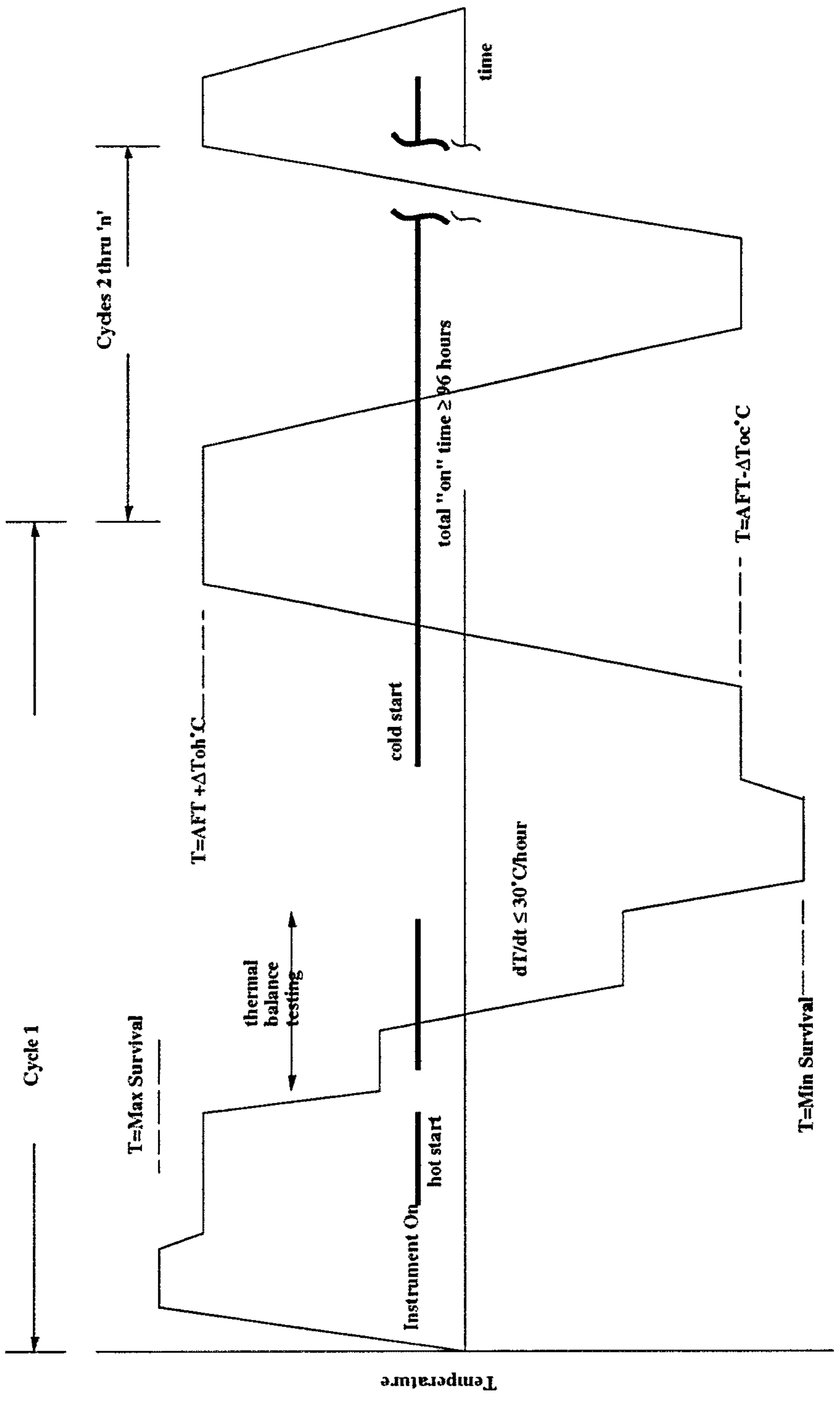


Figure 4.4-1 Model Thermal Vac Profile for Protoflight Testing

4.4.4.1 T -Vac Test Constraints

Instruments that must test multiple components should have fixtures and test control elements that allow each component to operate at its required test temperature simultaneously.

R-4.20: A comprehensive functional test shall be performed prior to TV testing to establish a baseline and again at the conclusion of testing.

Additionally, a comprehensive functional should be performed during at least one low and one high temperature soak. The comprehensive functional test should exercise all primary modes and all redundant assemblies or interfaces.

For instruments utilizing High Voltage power supplies the test procedure needs to address the operational scenario for those supplies.

Careful monitoring of the temperatures of critical assemblies is necessary to assure that they are not taken beyond their limits.

R-4.21: Components shall be instrumented to assure that critical assemblies are within their designated limits prior to application of power during T-vac. Monitoring thermocouples need to be attached to the instrument component in sufficient number and at such locations as required to determine critical temperatures. Locations of these thermocouples shall be recorded. Critical temperatures shall be monitored at all times and linked to an alarm system if necessary.

During hot and cold starts, temperatures must be stable (rate of change ≤1°C/hr.) prior to application of power.

R-4.22: Other than the initial start-up on the first hot cycle and the cold start test, the instruments shall remain operational during all transitions and key housekeeping parameters monitored and recorded at regular intervals.

Transitions may begin after the completion of the functional or temperature stabilization plus at least 6 hours, whichever is greater.

4.4.4.2 Facility Requirements

The facility selected for the TV test must meet the following minimum standards. (Further constraints may be added by the design team.)

The T-vac test chamber should be able to reach 1E-6 torr after initial outgassing and the chamber shall be of sufficient size so that the thermal characteristics of the components under test do not preclude the establishment, or maintenance of the required test temperature.

The following steps shall be taken to prevent contamination during T-vac:

1) the facility shall include a cryo panel which is active throughout the test;
2) a TQCM shall be used to monitor contamination;
3) other devices to measure contamination such as TQCMs, RGAs, mirrors, wipes, etc. may also be needed and;
4) the test should always start with a hot soak and end with a hot soak.

4.4.5 Thermal Balance

A thermal balance test supports the third objective discussed above, that is, a verification of the thermal design in a simulated flight environment. (A thermal balance test will also be done at the observatory level.)

R-4.23: Verification of the thermal model shall take place at the instrument or component level. A thermal balance test shall be performed on all instrument components which are thermally isolated from the spacecraft deck.

In general, a thermal balance test should be incorporated into the thermal-vac test as illustrated in figure 4.4-1. Instrument teams and their thermal engineer should work with Caltech on the test plan, test procedure, and facility requirements.

4.5 Thermal Models & Design data

R-4.24: A thermal model of the instrument component(s) that uses interface temperatures defined is section 4.1 and meets the prediction margins of section 4.2 shall be developed, presented in preliminary form at the PDR and in final form at the CDR or IR. The model shall be verified and documented in the IDDP and placed under configuration management after S/C CDR.

As described in Section 2.1 , all test results on flight hardware will be summarized in test reports which will also be contained in the IDDP.

4.6 Observatory Level Tests

A system level thermal vac test will be performed after all instruments have been integrated. The profile of that test is described in the APL Environmental Specifications Document APL 7345-9007.

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5.0 Electromagnetic Compatibility

The electromagnetic compatibility program for the ACE payload will be based on time-tested design requirements and a carefully selected set of tests that should assure a minimal probability of intra-instrument or instrument to S/C interference once the observatory is integrated. Too often, good EMC design practices are not followed and subsystem level tests are skipped, which basically assures that any problems, should they occur, happen at a point in the schedule where it is most expensive and most compromising to the delivery schedule. *Our approach will be to emphasize good design practice coupled with strict interface configuration management.* The test phase, at the instrument level, exists only to validate the design and assure readiness for integration. Caltech will provide support to all investigator teams without a specific EMC specialist and act as a coordinator for interface information.

5.1 Design Requirements

5.1.1 Grounding

R-5.1: Instruments shall provide Caltech with a detailed grounding diagram. The preferred grounding technique brings both the instrument primary and secondary grounds back to the S/C single point ground.

The grounding diagram needs to include the following information:

1) an indication of the method and location of ground for the secondary side of the main power converter;
2) an indication of the method and location of the ground for any high voltage supplies;
3) for instruments having more than one component, a schematic of the relationship between the signal and power grounds for each component, as well as harness configuration for intra-instrument cabling;
4) indication of the type and location of shield grounds for intra-instrument cabling;
5) any distinctions between digital and analog grounds;
6) input impedance of all interface filters and feed-thru's;
7) an indication of any "options" that exist in the grounding implementation;
8) notation of any elements of the instrument chassis which "float" with respect to other elements.

R-5.2: All instrument components shall be bonded to the S/C chassis by use of a ground strap to achieve a DC impedance $\leq 25\text{m}\Omega$

R-5.3: Instruments which isolate secondary common from chassis shall have a resistor installed between secondary return and chassis to ensure a bleed path for ESD when the instrument is disconnected from the S/C or GSE. 20 MΩ is suggested but this value may be altered depending printed circuit board capacitance and other factors.

Caltech will evaluate all grounding methodologies and offer alternative suggestions where appropriate. Both Caltech and APL shall have signature authority on the grounding diagram (at the "reviewed by" level). There are many "design rules" for grounding and as many reasons for breaking those rules depending on the circumstances. Therefore, we offer no specific requirements other than a thorough evaluation of the grounding technique coupled with tight configuration management. Any issues that conflict with specific S/C requirements will be dealt with on a case by case basis and documented in the SIIS.

5.1.2 Frequency Control

R-5.4: All instruments shall provide Caltech with a list of all internal clock frequencies and oscillator frequencies, an estimate of the accuracy and/or drift of that frequency with time/temperature, and an estimate of the rise time. Additionally, all instruments shall provide Caltech with a list of any frequency or band of frequencies to which they are known to be sensitive. A preliminary version of this list shall be provided at PDR and a final version at CDR or the Inheritance Review.

Caltech will keep this frequency database as up-to-date as possible and work with all instrument and S/C teams to assure that sensitive bands remain free of possible interference.

5.1.3 Intra-Instrument Cabling and Interface

Cables between instrument components are classified as either "quiet" or "noisy". All power and pyro signals are considered noisy. All "information-carrying" cables are classified as quiet. In general, cables of these two classifications should originate from two separate connectors and should be separately shielded. Other requirements and recommendations include:

R-5.5: Interfaces between instrument components with separate power converters shall provide a well-defined return path for all power and signals and that path shall be isolated from chassis.

R-5.6: Power supplied from one component to another shall be by twisted pair of the appropriate gauge and all current shall have a single (non-chassis) ground path back to the power converter.

R-5.7: Cables (with exception of S/C 28V primary power) shall have an overall shield and the termination of that shield shall be described in the grounding diagram discussed in Section 5.1.1. Connectors on cables with an overall shield shall be the type which provides for 360° (crimp ring) termination of the shield.

Analog interfaces between instrument components (with exception of non-critical housekeeping signals) should be differential.

Analog signals carried in the same cable bundle with digital signals and *not having separate shielding* (unless the analog signals are of a non-critical housekeeping nature) should have a EMC analysis done to determine couple noise levels and sensitivity of the receiver circuit to that noise.

5.1.4 Instrument Power Supply Specifications

R-5.8: Power converters either designed or purchased for instrument components shall be compatible with the S/C power subsystem and shall meet conducted susceptibility and conducted emissions requirements described herein. The supply must operate nominally for the power bus quality spec defined in 5.1.4.1 and must survive without degradation the fault bus spec defined in 5.1.4.2

The following specifications apply to all instrument power subsystems:

1) Primary to secondary common isolation must be greater than 1 MΩ;
2) To help assure adherance to the conducted emission spec (Figure 5.2-1)--
    - Limit capacitance between primary inputs and case ground to less than 0.1µf;
    - Balance capacitance between primary +28 and case and between primary return and case to 5% or better;
3) Turn on transients shall be limited to 2 amps (for instruments with currents less than 1A) or 2 times steady state current (for instruments with currents greater that 1A) and have rise times ≤ 2E4 A/s (see APL 7345-9005 for details);
4) Suppression circuits must assure that turn-off transients do not damage relay contacts (see APL 7345-9005 for details);;
5) Converter frequencies should avoid multiples of 30kHz and should be above 50kHz for new designs;
6) Power converters shall meet Mil-Std 461C CE01, CE03 and CE07 (modified according to Figure 5.2-1 and Figure 5.2-3) for conducted emissions and CS01 / CS02 (modified according to Figure 5.2-4) and CS06 for conducted susceptibility.

5.1.4.1 S/C Power Bus Nominal Power Quality Spec

Power bus voltage will be 28v ±2% under nominal operating conditions. Power bus ripple will be of $\leq$ 350mV pp within a 100MHz bandwidth. (It meets Mil Std 461C CE01/03) Repetitive spikes will be $\leq$ 0.5Vpp amplitude and short duration aperiodic transients are limited to a peak value of 3 times the bus voltage, with a maximum impulse of 1.4E-4 volt-seconds and a total duration of $\leq 1.7\mu s$. Modifications to the Mil Std 461C curves shown in Section 5.2.1 are consistent with these specifications.

5.1.4.2 S/C Power Bus Fault Clearing Mode

Fault clearing can be bring the bus to the battery voltage (approx. 18.9v) for up to 10 seconds. As part of load removal during fault recovery, the voltage can surge to 38 volts for up to 15ms. During ground tests and integration there exists the possibility of faults that produce a bus voltage anywhere between 0 and 30v for up to two minutes. Details of the Spacecraft power bus specification can be found in the GIIS (APL 7345-9005).

R-5.9: Instruments shall be designed to survive S/C bus fault conditions without degradation. (See the ACE GIIS APL-7345-9005 for details.)

5.1.5 Magnetic Field Control

In order to provide a minimum background magnetic field for magnetometer measurements the S/C and payload will emphasize certain engineering practices coupled with magnetic "sniffing" in certain cases. The largest contributions to a variable background field are the solar arrays, however, each payload element that uses magnetic materials, allows current to flow on unintentional paths, or uses improperly wired heaters can also make significant contributions to this undesirable background field. Rather than set down a single requirement for the field at the instrument and then "sub-allocate" that requirement down to the instrument or component level, the project has elected to assist each team in incorporating the right design practices, and using the proper materials and procedures that will minimize the stray fields from each component. Where a particular component is believed to be problematic, GSFC or Caltech may provide for "sniffing" and degaussing prior to integration. Decisions regarding this will be made jointly between the instrument team, Caltech, and the Magnetometer team. *In particular, all instruments will be "sniffed" as part of a routine acceptance process when delivered to APL for integration.* Several requirements and recommendations follow:

R-5.10: Select operating frequencies that avoid frequencies (fundamentals or harmonics of fun-

damentals) in the bands $f_n \pm \Delta f$ where f_n=15 kHz, 30 kHz & 60 kHz and Δf=200 Hz.

Avoid using magnetic "latching" relays and compensate all permanent fields;

R-5.11: Use heaters which are wired in such a way as to minimize the stray field;

Use non-magnetic materials when possible (connectors, electronics packaging etc.) and follow the basic grounding procedures required by this document;

Avoid the use of "soft" magnetic materials whose stray field can vary with time;

Use circuit board layouts that minimize the loop areas, especially on power supply boards;

Always twist power pairs between components and twist signal conductor pairs where possible;

Cooperate with the MAG team in providing them lists of possible magnetic sources and allowing them to visit your facility and "sniff" the instrument when appropriate;

Be aware of materials that can become permed during vibration testing.

Caltech will provide assistance to instrument teams in incorporating good design practices that support the magnetometer measurements.

5.2 Test Requirements

Prior to the pre-ship review all instrument components must have completed a minimal set of EMC tests. The instrument test matrix/test plan shall describe all tests that are performed and at what assembly level those tests are performed. Since there are no plasma wave receivers on board this particular S/C, the emphasis in the selection of tests has been based on the minimal set required to ensure compatibility with other S/C and payload hardware.

5.2.1 Emissions

R-5.12: Payload hardware (when tested under the specified configuration) shall not emit signals above the levels specified in the conducted emissions tests described herein.

5.2.1.1 Conducted Emissions

The following tests are to be applied to power cables only. Both differential and common mode tests (which include both primary and secondary return when applicable) are performed on the S/C to instrument power interface. Only the common mode tests apply to intra-instrument interfaces.

R-5.13: CE01--Narrowband Conducted Emissions from 30Hz to 15kHz:Tests shall be performed according to procedures described in Mil-Std 462 and the differential and common mode emission levels shall not exceed those illustrated in Figure 5.2-1 .

R-5.14: CE-03--Narrowband Conducted Emissions from 15kHz to 50MHz: Tests shall be performed on specified cables according to Mil-Std 462 procedures and differential and common mode emissions shall not exceed those illustrated in Figure 5.2-1 . (Tests for broadband emissions will only be performed if APL/Caltech EMC engineers determine a need. When applicable, those specifications in the APL Environment Spec 7345-9007 shall be used)

R-5.15: CE-07--Time Domain Transients: Using a LISN (specified in Figure 5.2-2) to simulate the S/C power bus, tests will be performed according to Mil-Std 462 procedures to determine, spikes and switching transients generated by the instrument or instrument component. For CE07A, Repetitive spikes should not exceed 0.5 volts (peak to peak) with a duration less thean 50μs. Ripple shall not exceed 350 mV peak to peak in the 30 Hz to 100 MHz bandwidth. Time domain switching transients (CE07B) shall not exceed those levels indicated in Figure 5.2-3 .

R-5.16: For instruments having multiple components powered by one primary supply, all of those components shall be operating during the EMC tests or shall at least be represented by an equivalent load. Instruments or components having multiple power configurations shall be tested at representative configurations.

It is recommended that, when procuring a DC-DC converter from a manufacturer who cannot supply data showing compliance with the above test requirements at the expected load and operating voltage, these tests be completed at the power supply assembly level on an engineering unit prior to committing to the flight power assembly design.

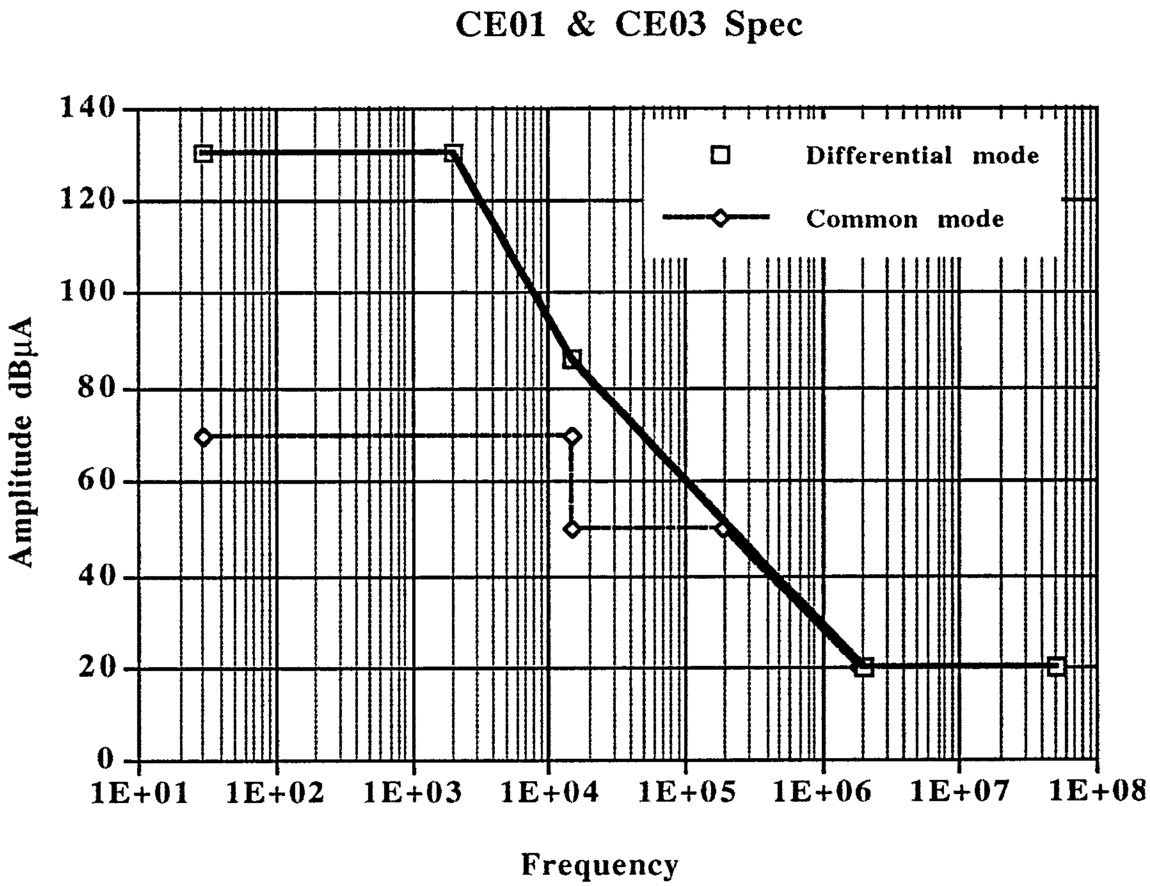


Figure 5.2-1 Conducted Emissions Specification for DC power leads

Figure 5.2-2 S/C power supply LISN for use with CE07 testing

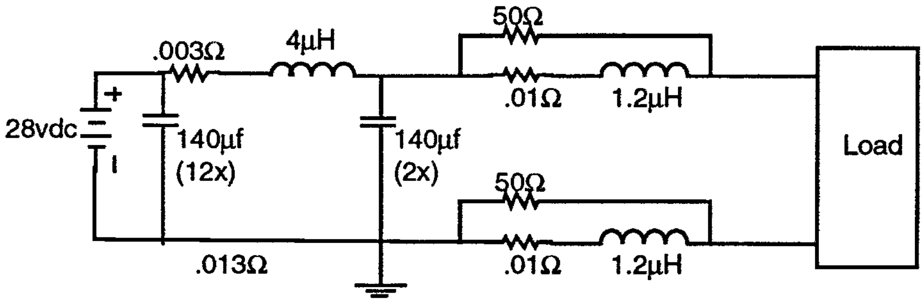
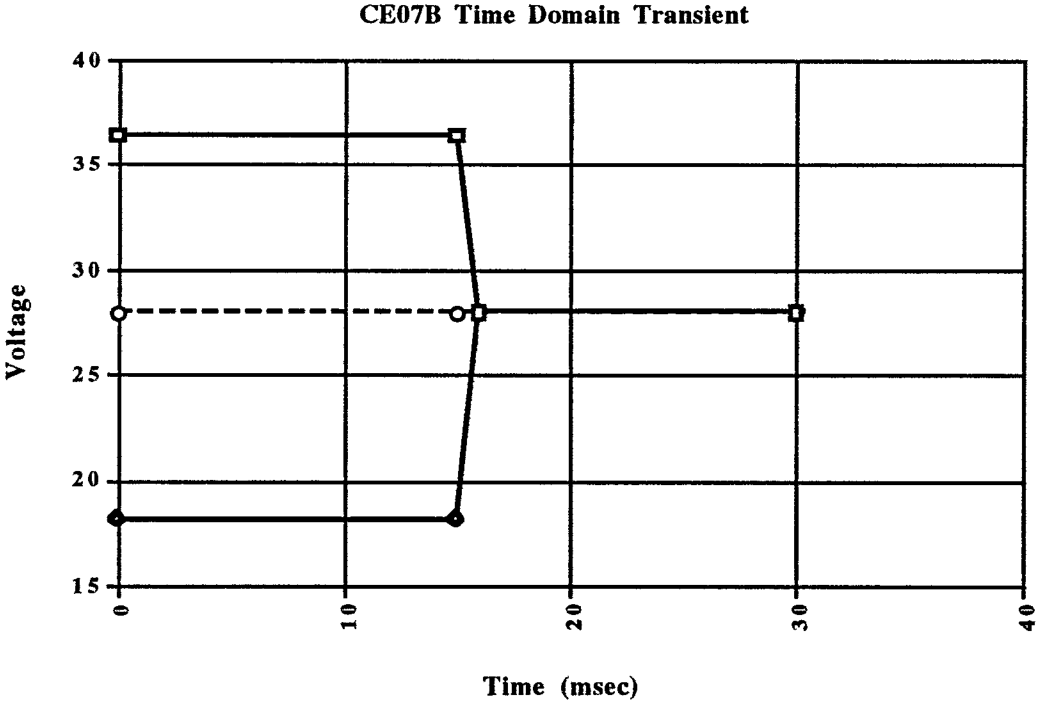


Figure 5.2-3 CE07B Modified allowable transients



5.2.1.2 Radiated Emissions

For instruments where grounding and/or shielding requirements discussed herein have been met, no radiated emissions testing will be required. *Caltech may, after reviewing the EMC record of inherited instruments, or after determining that a particular frequency internally generated by an instrument component is in the sensitive band of another observatory component, require a particular test.* In particular, instruments using frequencies above 50 MHz or frequencies in the 2025 to 2108 MHz band will be candidates for RE02 tests. The RE02 limits described in the the APL spec (7345-9007) shall apply. Likewise, instruments generating frequencies in the magnetometer "keep out bands" described in Section 5.1.5 may undergo magnetic "sniffing" in liu of a formal RE01 test. Determination of the need for RE testing will generally be made as part of test matrix development activity..

5.2.2 Susceptibility

5.2.2.1 Conducted Susceptibility

Susceptibility testing will be limited to 28v main power lines.

R-5.17: Completed instruments shall be capable of operation without degradation when subjected to the CS01 / CS02 tests at the levels indicated in Figure 5.2-4 and according to Mil Std 462 procedures.

R-5.18: Completed instruments shall have input power lines tested to CS06 modified(spikes) and shall be capable of continuous operation. The CS06 Spike to be used is 28v (on top of the nominal 28v) for a duration of 15 μs.

As with the conducted emissions testing, it is recommended that these tests be completed at the power supply assembly level prior to integrating the unit into the flight instrument so that any problems can be found early.

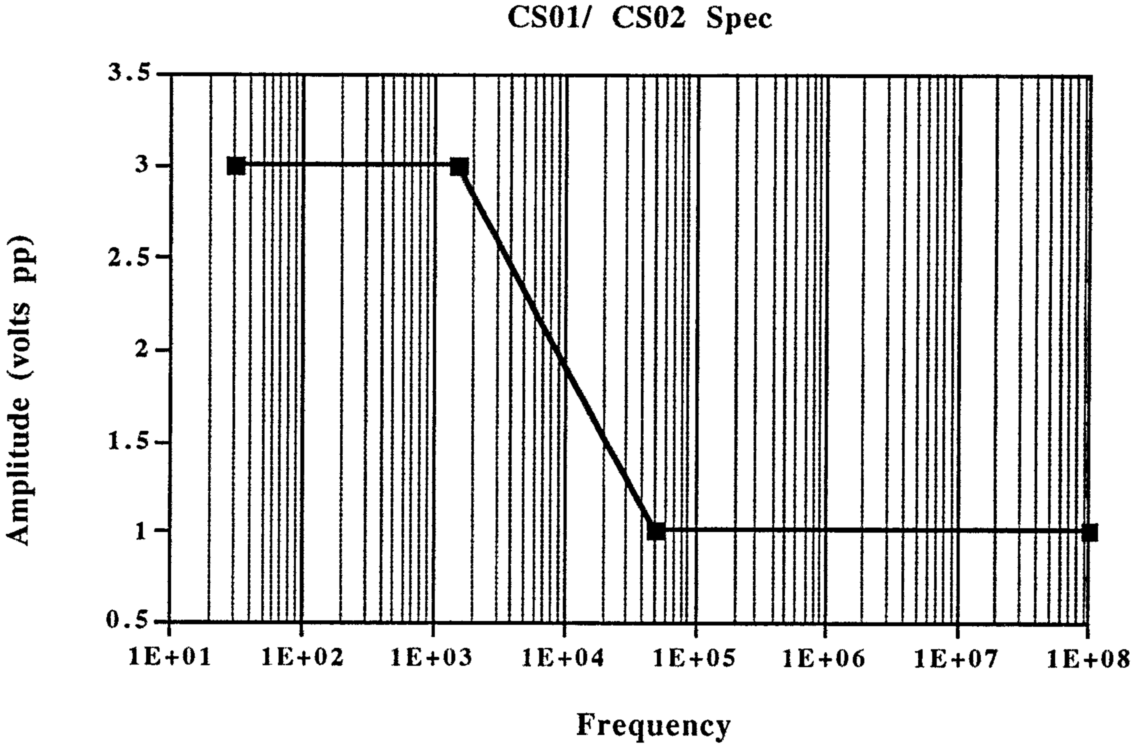


Figure 5.2-4 Conducted Susceptibility Spec for input power lines

5.2.2.2 Radiated Susceptibility

No radiated susceptibility testing is required. Should a particular component be suspected of susceptibility to the S/C transmitter, Caltech will work with that instrument team to assure compatibility on a case by case basis.

5.3 Observatory Level Test Program

EMC testing conducted at the observatory level is summarized inTable 5.3-1 . All testing will be based on Mil-Std 462 procedures. Having completed the above testing for all instrument components, the system level test is not anticipated to uncover any instrument compatibility problems. Instrument engineers should be available to support observatory level tests, however, since this is the opportunity to prove that the instrument functions nominally when all other loads on the bus are also active. Caltech and APL will assist instrument teams in finding the source of (and fixing) any interference that may be discovered during these tests.

Table 5.3-1 Observatory EMC testing

Test	Applicability
CE01	no
CE03	no
CE06	determined by subsystem test results
CE07A	primary power, power control
CE07B	primary power, power control
CS01	no
CS02	no
CS06	no
RE02	yes, tailored to launch env.
RS03	yes, tailored to launch env.

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6.0 Radiation

This section provides information on the naturally occurring space radiation environments to which the ACE payload will be exposed. The radiation environment for the ACE mission is relatively benign (by comparison with many other missions) but has the disadvantage of being non-deterministic. The environment is dominated by solar energetic particle events whose frequency and intensity are statistical in nature and vary with solar activity. Caltech and APL have used the latest statistical models to determine the environments for the ACE L1 orbit. Both the total dose and SEE environments are, therefore, probabilistic in nature. We have chosen guidelines for part selection and shielding which we believe are a reasonable compromise between cost and risk and make recommendations based on that balance. Should an instrument designer wish to depart from those guidelines, the information presented here, together with analysis assistance from Caltech PMO can be used to assess the risk associated with electing different design criteria.

Most of the radiation expected for ACE will likely occur during the solar active period which will begin in mid 1999. Therefore, designing for the minimum requirement of a 2 year mission vs. designing so as not to preclude the use of an instrument over a full 5 years is quite different.

R-6.1: All ACE payload elements shall be designed so as not to preclude the operation of an instrument for a full five years.

Since radiation can limit the useful life of space hardware, the five year design goal has been accounted for when specifying these environments.

6.1 Total Dose

Total dose affects electronic components by both ionization and displacement damage and can, at high enough levels, also effect certain material properties.

R-6.2: The radiation environment definition and design considerations shall apply to all ACE payload hardware, both new and inherited.

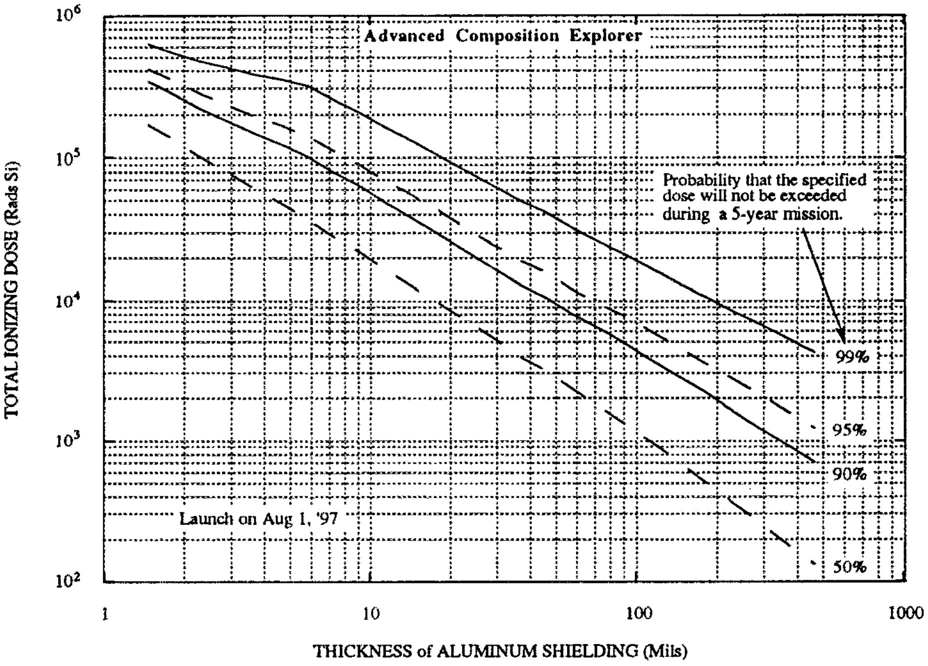
The concept of radiation design margin which is often used as a measure of part reliability is inapplicable in this case because of the statistical nature of the environment, therefore environments are given in terms of “probability not-to-exceed.” Any additional margin applied to that environment should account only for statistical variation in lot hardness of a part. The Caltech Electronic Parts Engineer can provide guidance with parts selection on a case by case basis.

6.1.1 Environment

The total ionization dose in Rads Si as a function of shielding thickness is given in Figure 6.1-1 . Shielding assumes spherical shell aluminum. The probabilities are for a full 5 year mission with launch in August of 1997 and represent a probability that the given dose will not be exceeded. Solar Proton fluence is calculated using the Feynman/JPL model (latest version) and dose is calculated using the NOVICE radiation code.

Figure 6.1-1 Total Dose Environment as Function of Shielding

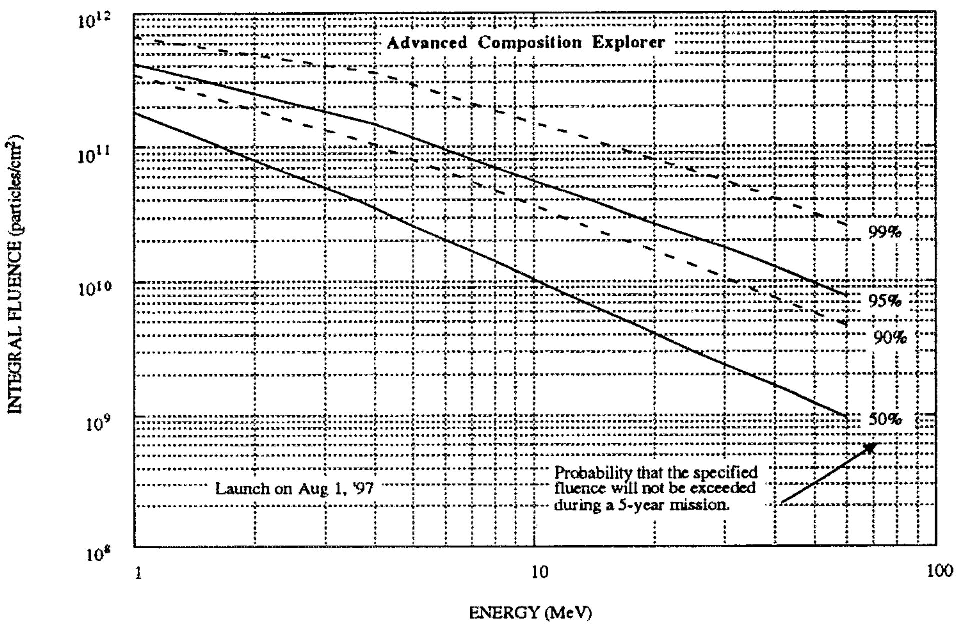
(assumes spherical shell)



For purposes of assessing displacement damage in detectors or sensitive components Figure 6.1-2 gives integral fluence probability curves for protons.

Figure 6.1-2 Integral Fluence Probability for Protons

(assuming an Aug.'97 launch)



6.1.2 Parts and Materials Considerations

As a guideline for electronic parts selection, instruments should select parts with an ionization dose capability greater than or equal to 10krad. (That uses the 90th percentile environment for a five year mission.) If the housing thickness is less than the assumed 60mil, consideration should be given to either using a harder part or increasing the effective shielding.

The parts and materials list supplied to Caltech by each instrument team will be reviewed by specialists and alternatives suggested where appropriate. *Where an electronic part, sensor or material can not survive this anticipated environment, Caltech can provide resources for spot shielding analysis and risk assessment.* Cost and schedule will be considered as part of this risk assessment.

6.2 Single Event Effects

Single Event Effects (SEE) are very important for the ACE payload because instead of just *surviving a particle event, much of the payload must remain operational during this period.* The Science Requirements Document states a number of "flare" related objectives and references the instruments needed to achieve each. Instruments whose data are needed to achieve Solar Energetic Particle Event (solar flare) objectives should assure that they remain operational (that is, the instrument can obtain sufficient data to achieve the objective) in the design case environment described below and, in case of any SEE that resets the instrument, can re-establish communication with the S/C C & DH subsystem.

Other instruments whose data are not required to achieve these flare related objectives must assure that they do not suffer any anomaly that is unrecoverable and that their performance does not degrade as a result of the design case particle event.

R-6.3: All instrument designers shall assure that, in the case of a "watch dog" reset resulting from a SEE, the instrument can restore itself to a "safe" condition.

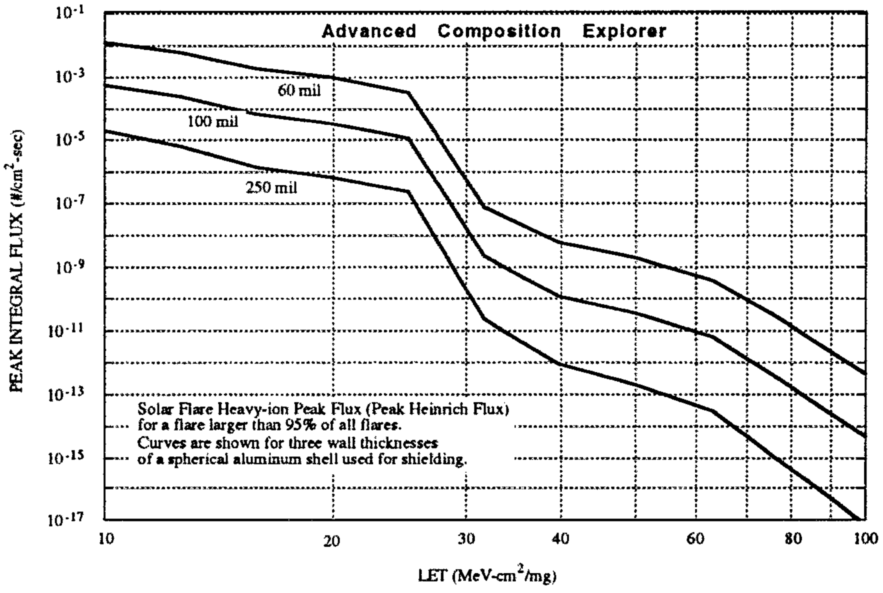
Caltech can provide assistance in designing circuits and software which are immune to SEE.

The design environments described here represent the latest, most realistic models available for solar particle events. They are also statistical in nature, therefore we select a "design case" event which has only a 5% chance of being exceeded. Descriptions of the model methodology are available upon request.

6.2.1 Design Environment

The design case environments are described by the Heinrich Flux (the Integral Flux as a function of LET) behind various thicknesses of aluminum shielding. Figure 6.2-1 and Figure 6.2-2 specify peak event flux and event fluence respectively. The peak flux should be used to calculate peak upset rates. Peak fluxes can be effective for minutes to hours. The Heinrich fluence can be used to calculate the total number of upsets over the period of the event (assume an event duration of TBS if you want to know an "average" rate).

Figure 6.2-1 Ordinary Heinrich Peak Flux for Design Case Event



Solar Flare Heavy-ion Peak Flux (Peak Heinrich Flux) for a flare larger than 95% of all flares.
Curves are shown for three wall thicknesses of a spherical aluminum shell used for shielding.

Figure 6.2-2 Heinrich Fluence for Design Case Event

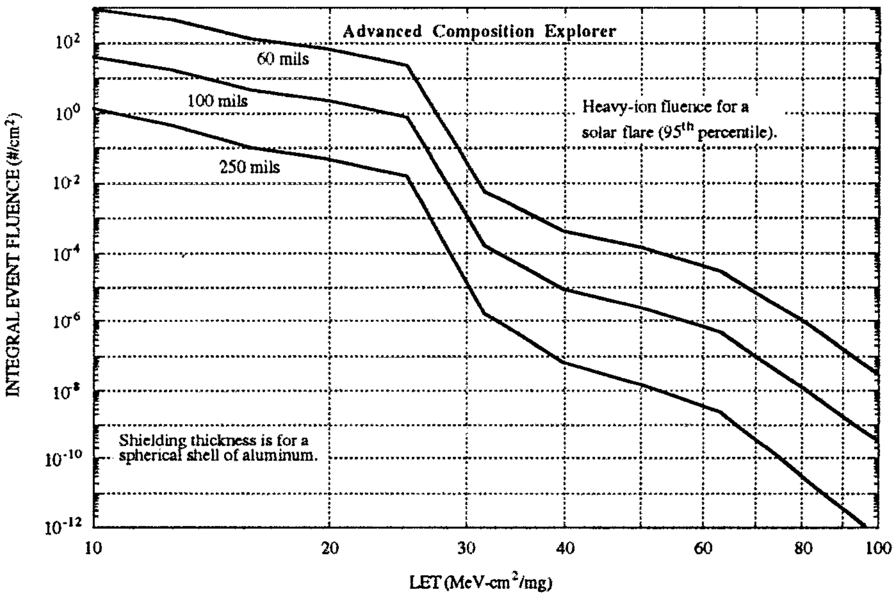
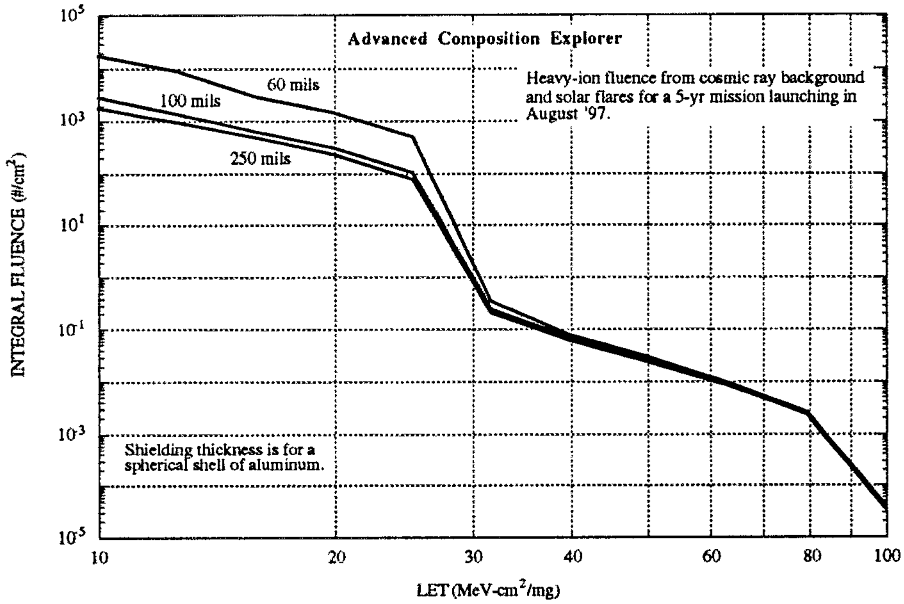


Figure 6.2-3 gives the shielded Heinrich fluence of high LET particles for a five year period. This consists of GCR plus the 95th percentile solar environment for an August'97 launch. For electronic parts which are known to be susceptible to latch-up, their latch threshold coupled with their latch cross-section should be used with these fluences and Poisson statistics to calculate the probability of latch-up.

Figure 6.2-3 Heinrich Fluence for High LET particles



6.2.2 Guidelines for SEE immunity

The following requirements and guidelines should be followed during the design process to help assure operability during, and survivability of, these energetic particle events:

1) Select electronic parts which are immune to latchup;

2) If a part is not immune to latch-up, first analyze the latch-up probability in the design case environment given above by using measured (or estimated) latch-up cross-sections and Poisson statistics, second, assess the ability of detecting and resetting the latch-up (Caltech can provide assistance) and the impact of latch-up (permanent degradation vs. momentary data interruption), and third, explore the selection of an alternate part;

3) For single event upsets, first analyze the peak upset rate by using the design case environment given above, second, determine how the upset may be detected, and assure that the impact of such an upset does not impact the experiment objectives. *The instrument Co-Investigator is the ultimate arbitrator for deciding whether any loss of data is acceptable;*

4) Do not select parts with a SEU threshold less than an LET of $\approx$13 Mev cm^2/mg. These parts can be susceptible to proton upset as well as heavy ion upset making rate calculations increasingly difficult and prone to error.

5)

R-6.4: Conduct a FMEA on all S/C interfaces to assure that any single event effect occurring in a instrument component cannot propagate across the S/C interface.

Caltech will provide support for any of the above analyses at the instrument developers request.

6.2.3 Part Data

All instrument part lists will be reviewed for SEE immunity by Caltech. Project engineers will be alerted regarding susceptible parts and Caltech will work with instrument teams to assess the risk associated with use of the part and, if necessary, select an alternative. Questions regarding the sensitivity of any part under consideration should be directed to the Caltech performance assurance manager. Any data available on the part in question will be supplied.

7.0 Ground Environments

7.1 Handling and Storage

R-7.1: Flight hardware shall always be protected from exposure to natural or induced environments that could cause degradation. Flight hardware shall be maintained within the environmental qualification test limits that are specified for the hardware element being stored.

Protection from environment limits beyond the scope of testing in the normal environmental qualification program must be based on analysis which results in a specification that defines both the hazard and method of protection.

R-7.2: Flight hardware elements must be maintained in areas that afford protection from theft, temperature extremes, fire, water, humidity, contamination, electrostatic discharge, and earth quake.

Flight hardware storage should be kept in an areas with controlled access. The temperature should be kept to within temperature limits determined by the most thermally sensitive instrument assembly. Storage areas should be located within a facility that is resistant to fire. Equipment should be protected from sources of water, such as roof leaks and fire sprinklers. The same level of humidity controls that are used on an assembled instrument, such as purging for the protection of detectors, should be employed on humidity sensitive devices that are in flight stores.

R-7.3: Contamination controls shall be maintained at the levels specified in ACE-CT-100-23, "Contamination Control Plan for the Advanced Composition Explorer Payload."

Contamination controls to be considered include: maintaining a clean room environment in all assembly and test facilities; bagging instrument elements; storage in dust proof cabinets; and storing the instrument in its transportation carrying case, which may be maintained under continuous GN_2 purge. All parts and assemblies that are vulnerable to electrostatic induced damage should be protected by being kept in containers that provide ESD protection. In areas that experience earth quakes, flight hardware should be protected from seismic induced damage. Seismic protection considerations should include: tethers or containment to prevent falling; ensuring that loose articles cannot fall on the flight hardware; and that tipping cabinets or fixtures cannot spill out or tip over on flight hardware.

7.2 Shipping

R-7.4: Flight hardware being shipped from one facility to another must be protected from damage that could be caused by: temperature extremes, shock and vibration, humidity, contamination, and electrostatic discharge.

Care must be exercised when packaging flight hardware for shipment and handling the hardware during the transport. When hardware is being shipped via air transportation it is strongly recommended the that the equipment be carried within the aircraft passenger cabin. If it is not possible to carry flight hardware within the passenger cabin, the hardware should be escorted through the loading process; the flight should be direct; and the aircraft should be met at its destination.

R-7.5: During shipment the temperature must be kept to within survival temperature limits or more stringent limits defined by other factors such as relative humidity, contamination etc.

Many "common sense rules" apply, for example, the hardware should not be exposed to direct sunlight.

R-7.6: Flight hardware must be protected from excess shock and vibration. The packaging must be designed so that the hardware will be protected from shock and sinusoidal vibration levels that are specified by the experiment design team, when the acceleration levels specified in Table 7.2-1 are imposed on their containers.

These acceleration levels are typical for commercial trucks and aircraft with proper placement and securing of the containers within the vehicle. Desiccants should be packaged within shipping containers to protect flight hardware from moisture if a dry nitrogen purge is not used. Flight hardware, such as solid state detectors, that is particularly vulnerable to damage from moisture should be protected by employing a GN_2 back fill and sealing the containers.

R-7.7: Care must be exercised so that the container is not over pressurized due to decreases in cabin pressure during air transport.

The selection of insulating and shock absorbing materials in containers should ensure that contamination and electrostatic charging are controlled.

Table 7.2-1 **Acceleration Levels for Shipping and Transportation Vibration**

Frequency (Hz)	Acceleration Level (G_{peak})
5 to 35	1.3
35 to 48	3.0
48 to 100	5.0

7.3 Integration and Test Environment

7.3.1 JHU/APL

Upon arrival at APL, the APL integration team will provide a controlled temperature / humidity, clean environment, and make nitrogen purge available. Instruments with peculiar or very stringent contamination control needs should make sure those requirements are called out in the SIIS for the instrument. After acceptance by APL for integration on the S/C, the APL Contamination Control Plan (7345-9102) is the controlling document for all operations at APL and GSFC. This plan should be reviewed carefully by the instrument teams and any exceptions or issues identified in section 8 of the SIIS.

7.3.2 GSFC

During testing at GSFC the APL integration and test team will continue to provide nitrogen purge. for all test time except of course during thermal vac. The requirements called out in Section 4.0 of this document regarding the cleanliness of the thermal vac facility shall apply here as well. Caltech will be working with APL & GSFC to assure that the facility meets all of the requirements specific to certain instruments. Instruments should be sure to input these specific requirements to the Caltech Product assurance manager for inclusion in the Caltech Contamination Control Plan. Specific requirements on APL should also be documented in your SIIS.

7.4 Launch Site Environment Considerations

The launch site environment poses particular risks to some instruments sensitive to contamination, radio frequency interference, humidity, etc. Caltech will be working with APL and

GSFC to help assure an environment that is “friendly” to the ACE payload. APL will supply purge up until launch as well as during shipment to the cape. Caltech and APL should be informed of instrument-specific needs so they may be included in the control plan and instrument SIISs.